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Design of Micropower Microphone and Speech Detection Circuits

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Abstract

This thesis describes the design of a low-power speech detector chip. It will be used between an electret microphone and a microcontroller and will generate a digital wake-up signal for the microcontroller when the audio signal is sufficiently "speech-like" to initiate higher-level processing of the amplified audio signal. The rest of the time, the microcontroller will sleep and consume nearly negligible power. The system is implemented using mostly low-power analog continuous-time subthreshold circuits. The speech detection method is based on a model simplified from Büchler. It detects speech by measuring the total modulation spectrum power in the 2–16 Hz phoneme modulation band. It uses Baker and Sarpeshkar's low-power high-PSRR microphone preamplifier to amplify the microphone signal in the 100 Hz to 2 kHz speech band. The squaring nonlinearity in Delbruck's antibump circuit extracts the power in the speech band by comparing the amplified microphone signal with its average value. This current-domain power signal is filtered for the phoneme modulation power in the 2–16 Hz band by Mulder et al.'s first-order log-domain band-pass filter. Zhak and Sarpheshkar's class-B current mirror performs half-wave rectification of this modulation signal. Finally, Indiveri's low-power silicon neuron generates a spike train whose spiking frequency is proportional to the power in the phoneme band. The design includes Delbruck's on-chip bias generator for self-biased operation. The design was targeted at the 1.6 μm MOSIS TinyChip process but with a reduced power supply of 3.3 V. It uses 2 mm^2 of area. The average simulated power consumption at chip-level is 215 μW at a 3.3 V power supply including the microphone front-end and the bias generator, and 93 % of this power is the microphone preamplifier. The power consumption reaches a maximum of 475 μW when the silicon neuron spikes.

In addition, a microphone preamplifier with controllable feedback resistance for variable gain was designed for fabrication in the MOSIS 0.35 μm CMOS process for a future binaural silicon cochlea. Details of a standard electret microphone are shown. A detailed small signal analysis of Baker and Sarpeshkar's microphone preamplifier shows how the high-frequency rolloff is critically affected by the parasitic gate-to-drain capacitance of the adaptation feedback transistor.

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Chapter 1

Introduction

This project presents the design of a micropower speech detector using mostly continuous-time subthreshold analog circuits. It is used between a cheap electret microphone and a microcontroller and generates a digital spiking voltage whose spiking frequency indicates the likelihood of speech versus non-speech. The output signal is used as a wake-up signal for the microcontroller and the amplified microphone signal can be further processed with more powerful algorithms in the subsequent device. An analog-to-digital converter (ADC) might be used to digitize the amplified microphone signal at the output of the microphone preamplifier. The speech detector is supposed to be incorporated into a battery powered device, hence, a key figure of merit is the power consumption. The total power consumption will be an estimated 200 μW, allowing continuous operation with 2000 mAH AA batteries of more than a year. In this project, the design is finalized and laid out, ready for fabrication.

Another aspect of this project is to get a better understanding of cheap universally-employed electret microphones and in what kind of adaptive configuration they can be used to trade signal-to-noise ratio (SNR) and power consumption. The project is in the context of the Swiss National Science Foundation (SNF) project DollBrain [1] and partially builds on previous unpublished results obtained in the 2005 class design project.

1.1 Context of the Speech Detector

[1] describes that standard natural human-machine interaction that relies on vision and audition requires state-of-the-art technology that consumes tens of watts, making it impossible to run the necessary algorithms continuously under battery power. It would be advantageous to burn full power only when a human desiring interaction is detected. The DollBrain project is inspired by nature, where interactions among species require high effort and high energy consumption only for small intervals of time and at all other times, the organisms are in an idle state and watchful for stimulation where the efforts are low and the energy is conserved.

The DollBrain project aims at developing technology to address these issues by generating wake-up signals using micropower face and voice detection sensors. In this thesis, a speech detector is designed and novel ultra low power audio processing circuits are devised.

1.2 State-of-the-Art Micropower Audition

The hearing aid industry is an area where power consumption is critical and detection of speech/non-speech is very desirable [1]. Büchler [2] developed a sophisticated sound classification algorithm for hearing aids. In a first approach, a hearing instrument can classify the following five main acoustic situations: silence, speech, speech in noise, noise and music. However, these algorithms run on a DSP and burn typically about 1 mW on a state-of-the-art hearing aid. Therefore, a simpler approach is needed with a less reliable algorithm than can be implemented using subthreshold analog circuits. It is a promising field of interest because portable speech-recognition systems of the future will likely have more analog processing before digitization to reduce the computational bandwidth on the DSP and save power.

In [3], a low-power current-mode microphone preamplifier with a high power-supply rejection ratio (PSRR) has been demonstrated with a total power consumption of 96 μW (including the 60 μW of the microphone built-in buffer) and an in-band PSRR that varies from 60 dB to 90 dB. Wide-dynamic-range low-power microphone preamplifiers are used in bionic implants for the deaf for instance. It has been proved in literature that it is possible to build low-power front-ends without a loss in dynamic range and in-band PSSR, but the existing devices all suffer from a fundamental limitation: The microphone interface ends up burning much more power than the rest of the circuit [1]. It might be necessary for devices which aim at reproducing the speech signal that the microphone is biased with a high current in order to get a good performance in terms of PSRR and dynamic range, but for a simple speech-detection algorithm it is conceivable that the microphone runs at a much lower bias current level with a reduced sensitivity. In this way, an increased SNR is traded for lower power consumption.

As an example, HandiWorks advertises a key finder, which reacts to a three-clap pattern and emits several loud beeps and costs a mere 15 US dollars [4]. Its sensors have a 20-foot radius. It is powered by a single lithium long-life battery of about 25 mAH capacity and is claimed to result in a lifetime of two years. Such devices have been offered for at least 10 years, therefore, it should be possible to further evolve these methods and make the sensor even react to speech.

1.3 Prior Work

A behavioral model of the speech detection algorithm in MATLAB was previously developed by Delbruck based on a suggestion from Hynek Hermansky. It showed

acceptable performance in the context of the DollBrain project, which aims for detecting conjunctions of speech and face detection, and was chosen for implementation with subthreshold analog circuits. Previously, some subcircuits for this project have been partially developed in the Neuromorphic aVLSI course, but all of them except the microphone preamplifier needed redesign because they were erroneous and not documented. A microphone model was provided by Michael Baker, the author of [3].

1.4 Challenges

In this project, we face the following challenges:

- How to build low-power microphone interfaces.
- How to efficiently and cheaply classify speech/non-speech.
- How to efficiently implement this algorithm using dedicated ultra low-power circuits.
- How to respect the current or voltage modes at the interface of the different subcircuits.
- How to make a speech/non-speech decision and convert the current signal back into a digital voltage for the interaction of the speech detector with the microcontroller.

1.5 Algorithm

The computational effort and thus the power consumption of existing algorithms in literature [2] is too high. Algorithms with moderate reliability of detecting speech/non-speech are sought for most efficient implementation in dedicated circuits, where they can run continuously for extended periods on battery power.

A simple speech detector algorithm, which is capable of measuring the speech modulation power (phoneme band power), consists of amplifiers, first-order filters, rectifiers and comparators and measures the power in the speech band (see Fig. 1.1 (a)). This algorithm is based on suggestions by Hynek Hermansky, project partner, at the 2004 Telluride Neuromorphic Engineering Workshop.

The speech band signal in the range of 100 Hz–2 kHz results from broad-band filtering the microphone signal and is squared in the following stage to extract the instantaneous signal power. A band-pass filter measures the phoneme band power in the order of 2–16 Hz. The resulting signal is rectified before a low-pass filter averages the signal over time. The average phoneme power is compared with a threshold to make the speech/non-speech decision.

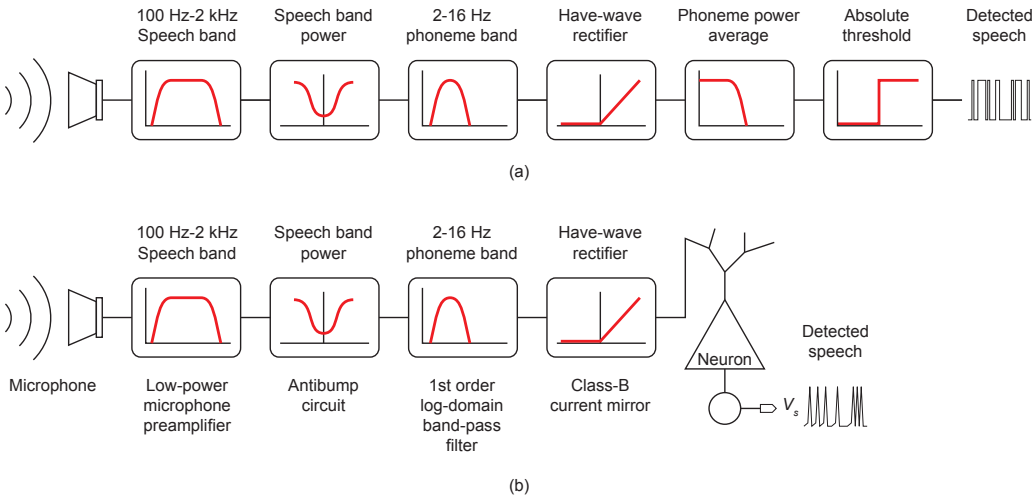


Figure 1.1: Speech/non-speech detection algorithm. (a) Original algorithm as proposed by Hynek Hermansky, partner in the DollBrain project. (b) Circuit architecture using dedicated subthreshold analog circuits.

In the speech detector architecture which will be presented in Chapter 3, the phoneme band power averaging filter and the comparator are substituted by a silicon neuron (see Fig. 1.1 (b)). The rectified current, which represents the phoneme band power, is injected into the neuron and averages the signal on the membrane capacitor. Once the membrane potential is higher than a given threshold, a spike (train) is generated.

We assume that speech close to the microphone is loud enough to make a comparison with an absolute threshold. However, loud non-speech signals or noise can erroneously be classified as speech.

1.5.1 Microphone Preamplifier

The AC microphone JFET buffer current signal is sensed in the microphone preamplifier and band-pass filtered. The voltage signal from the equivalent microphone input voltage source is amplifed to the output of the microphone preamplifier.

1.5.2 Power

It is crucial to make use of a nonlinearity to obtain the power of the signal because a nonlinearity demodulates the speech signal into the baseband. If we assume that the speech signal with the frequency ω_{mod} (e.g. 6 Hz) is modulated with a carrier signal of the frequency ω_{car} (e.g. 2 kHz), we get spectral components of the signal

at the sum and at the difference of the frequencies

$$x(t) = \cos\omega_{\text{mod}}t \cdot \cos\omega_{\text{car}}t = \frac{1}{2}\big(\cos(\omega_{\text{mod}} - \omega_{\text{car}})t + \cos(\omega_{\text{mod}} + \omega_{\text{car}})t\big) \tag{1.1}$$

Here, the demodulation is achieved by squaring the signal $x(t)$

$$y(t) = x^2(t) = (\cos\omega_{\text{mod}}t \cdot \cos\omega_{\text{car}}t)^2 \tag{1.2}$$

$$= \frac{1}{4}\big(\cos^2(\omega_{\text{mod}} - \omega_{\text{car}})t + 2\cos(\omega_{\text{mod}} - \omega_{\text{car}}) \cdot \cos(\omega_{\text{mod}} + \omega_{\text{car}})t \ldots \tag{1.3}$$

$$\ldots + \cos^2(\omega_{\text{mod}} + \omega_{\text{car}})t\big)$$

$$= \frac{1}{4}\left(\frac{1 + \cos\big(2(\omega_{\text{mod}} - \omega_{\text{car}})t\big)}{2} + \cos(2\omega_{\text{mod}}t) + \cos(2\omega_{\text{car}}t) \ldots \right. \tag{1.4}$$

$$\left. \ldots + \frac{1 + \cos(2\big(\omega_{\text{mod}} + \omega_{\text{car}})t\big)}{2}\right)$$

Not surprisingly, the modulation frequency of the power is doubled. Büchler [2] (pp. 16–17) proposes that the modulation frequency of clean speech is in the order of 2–8 Hz. This fact leads to a power modulation band of 4–16 Hz.

1.6 Organization of the Report

In Chapter 2, we give an overview of state-of-the-art electret microphones and present alternative approaches for microphone preamplifiers in future speech detection systems. In Chapter 3, we discuss the specifications and the design of the speech detector in detail and present chip-level simulation results of all major building blocks and the full circuit including the bias generator. In Chapter 4, we show how the layout of the circuit was carried out and focus on practical aspects of chip design. In Appendix A, we derive and analyze the transfer function of the microphone preamplifier from the equivalent microphone input voltage source to the microphone preamplifier output in great detail. Appendix B gives details required for chip testing.

Chapter 2

Electret Microphones and Microphone Preamplifiers

Microphones convert acoustic signals into electrical signals. Most microphones have in common a thin and light membrane that is actuated by air pressure [5]. The movement of the diaphragm is then converted into an electrical signal by means of different physical effects. We focus on electret microphones because they bring excellent performance at very low costs (less than 1 $ in volume) and are highly miniaturized (as small as 2 mm in diameter). Furthermore, they show an excellent low-noise characteristic and do not need high external polarization voltages and thus can be battery powered.

In this chapter, we give an overview of the working principle of an electret microphone and show how it can be interfaced by analog circuits. Since most electret microphones employ a JFET buffer to transform the signal voltage, the understanding of the JFET is essential. A short introduction to JFETs is given. Moreover, the design of a microphone preamplifier based on [3] with controllable feedback resistor is presented along with new approaches in audio amplifier design.

2.1 Electret Microphones

The big drawback of capacitor microphones is the requirement for high external polarization voltages [6]. Sessler invented a capacitor microphone which used an electret material as the movable diaphragm [7].

[6] describes that an electret is a prepolarized material, usually polytetrafluoroethylene, which has been given a polarization or permanent electrostatic charge through placement in a strong electric field and under heat. When the heat is removed, the electric charge or polarization remains. The same peformance characteristics as a standard capacitor microphone with a polarization voltage of about 100 V is obtained when an electret microphone with a polarized state-of-the-art electret material is used. Modern electret microphones usually require a 5-to-9 volt supply to power the integrated voltage buffer.

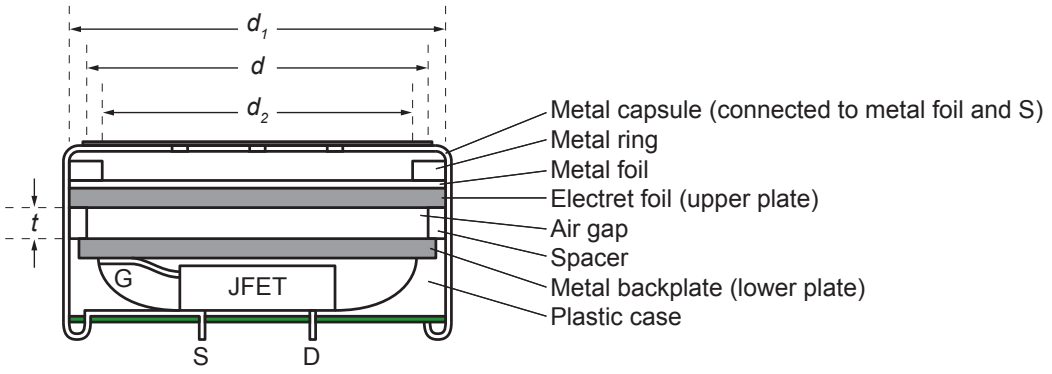


Figure 2.1: Typical cross sectional view of an electret microphone with a metallized electret foil and a JFET buffer.

Electret microphones come in two flavors: Electret microphones which have an electret diaphragm coated with a metal foil exist. Alternatively, capacitive microphones whose backplate is covered with an electret material are available. A disadvantage of the former configuration is that the metallized electret foil increases the mass per unit area of the membrane in contrast to the non-electret one. This might jeopardize the high-frequency response of the microphone [6]. The inexpensive electret microphones we purchased, however, all have a polarized diaphragm.

In the meantime, earlier material problems of electret microphones have been overcome and further improvements have come mainly in miniaturization, making the small electret microphone the standard device in almost every consumer and communication audio application. However, advancements of sensitivity, signal-to-noise ratio, linearity and supply current have not been achieved [8].

A cross sectional view and the parts of a typical electret microphone with a metallized electret foil are shown in Figs. 2.1 and 2.2, respectively. The most commonly used electret microphone contain a JFET inside the electret microphone capsule which builds a buffer between the capacitive sensor and the output. A JFET is a three-terminal device and incorporated into a small plastic package.

2.1.1 Junction Field-Effect Transistor (JFET)

A typical electret microphone uses a JFET as an impedance converter because it provides a good interface to the capacitive sensor. JFETs are depletion mode devices and, in the case of a n-type JFET, even conduct current for zero gate-to-source voltage due to a negative threshold voltage V_{t0}. This fact is beneficial in the context of electret microphones because it allows the operation of a nJFET at a reasonable operating point without a bias voltage between gate and source.

N-type JFETs consist of a P-doped gate and an N-doped channel. Since JFETs are bulk devices, which do not have a thin interface that can trap and detrap charge, they show an excellent low-noise performance and find application in electret

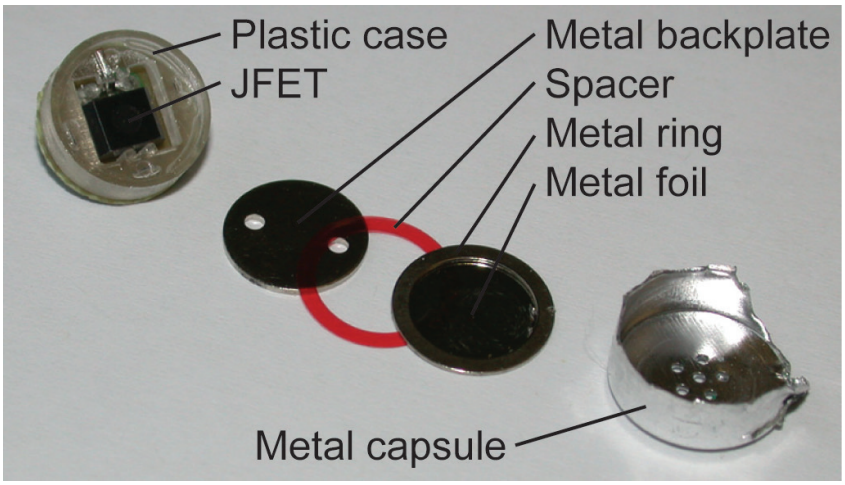


Figure 2.2: Microphone parts.

microphones.

The JFET large-signal model in T-Spice uses the basic FET model of Schichmann and Hodges [9] (pp. 365–367) and is shown in Fig. 2.3. It consists of a voltage controlled current source between the drain and the source and two diodes from gate to drain and gate to source. In reality, however, there is a distributed diode from the gate to the channel. During regular operation with $V_{gs} > 0$, the diode from gate to drain is reverse biased and the diode from gate to source is forward biased. The large-signal device equations for an n-type JFET are given by

$$I_{ds} = \begin{cases} 0 & \text{for } (V_{gs} - V_{t0}) \leq 0 \\ \beta(V_{gs} - V_{t0})^2(1 + \lambda V_{ds}) & \text{for } 0 < (V_{gs} - V_{t0}) \leq V_{ds} \\ \beta V_{ds}\left[2(V_{gs} - V_{t0}) - V_{ds}\right](1 + \lambda V_{ds}) & \text{for } 0 < V_{ds} < (V_{gs} - V_{t0}) \end{cases} \tag{2.1}$$

where the threshold voltage V_{t0} of an n-type JFET is usually in the order of -2 V. The gate-to-drain and gate-to-source leakage currents are

$$I_{gd} = I_{S1} \cdot \left(e^{V_{gd}/U_T} - 1\right) \tag{2.2}$$

$$I_{gs} = I_{S2} \cdot \left(e^{V_{gs}/U_T} - 1\right) \tag{2.3}$$

where I_{S1} and I_{S2} are the gate junction saturation currents in the order of 1.0×10^{-14} A, $U_T = kT/q = 25.4$ mV is the thermal voltage and λ is the channel-length modulation parameter.

The characteristics of a n-type depletion mode JFET for different gate voltages are depicted in Fig. 2.4. It is apparent that for $V_{gs} = 0$ a significant current of about 220 μA in saturation flows through the device.

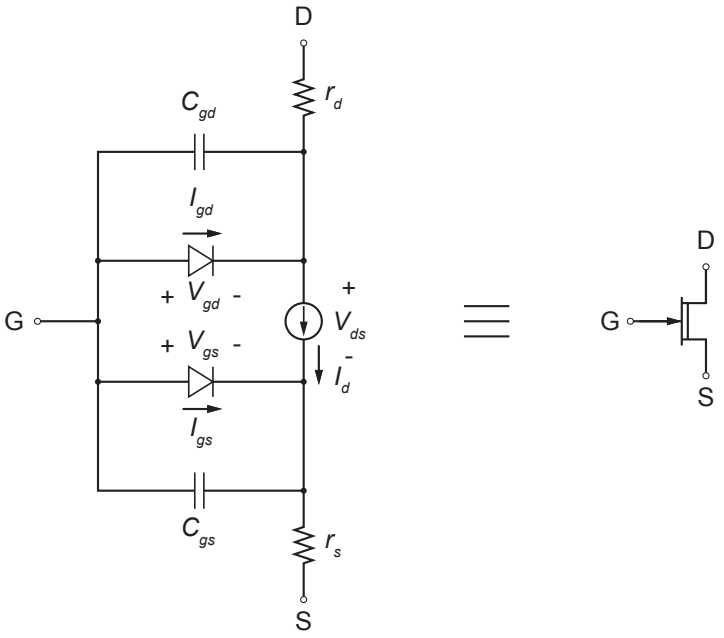


Figure 2.3: JFET model according to T-Spice specifications.

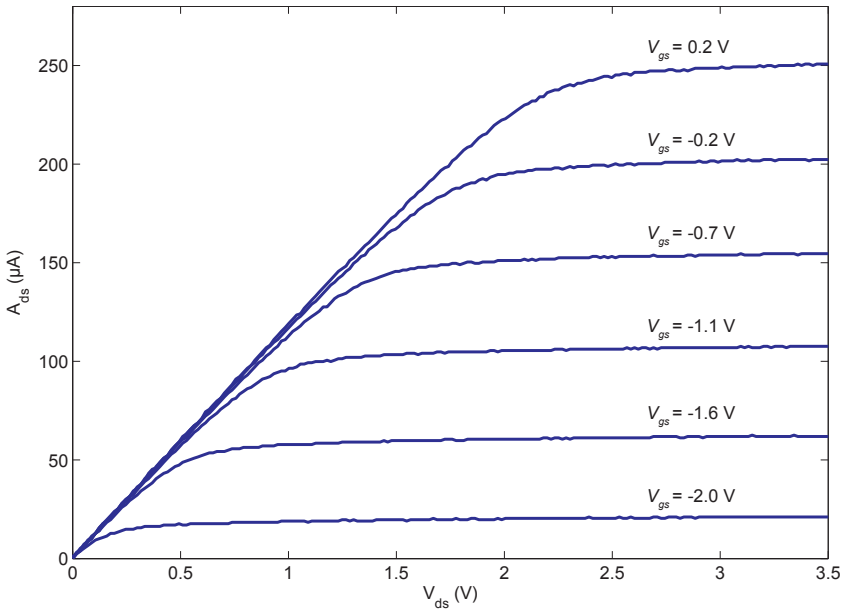


Figure 2.4: Measured I–V characteristics of a n-type depletion mode JFET (BF244A/B).

2.1.2 Self-Biasing of the JFET

In DC equilibrium at the gate of the JFET, there is no current flow through the capacitor and consequently the currents through the gate-to-drain I_{gd} and gate-to-source diodes I_{gs} must balance. Therefore, the DC voltage of the gate of the JFET settles around $V_{gs} \approx 0$ V. This analysis is only qualitative because the distributed diode between the gate and the channel is approximated by two lumped diodes from gate to drain and gate to source, respectively.

2.1.3 Working Principle of the Electret Microphone

A disturbance in the diaphragm due to sound pressure changes the microphone capacitance and creates a small-signal current from one plate to the other which in turn causes a voltage drop across the associated resistance of the reverse-biased diode of the JFET [7]. This voltage change is amplified by the transconductance of the JFET and transformed into an AC signal current which can be sensed by a subsequent amplifier.

2.1.4 Microphone Model

A complete microphone model (including the JFET) for use in T-Spice was provided by Michael Baker, one of the authors of [3] and is shown in Fig. 2.5. As described in [8], the electrical representation of a capacitive sensor consists of an equivalent small-signal voltage source v_i in series with a source capacitor C_{mic} (see Fig. 2.5). It is also pointed out that audio microphones need high-pass filtering with a cut-off frequency around 100 Hz to attenuate large low-frequency signals. Reportedly, the input impedance r_{in} of a typical JFET is around a few 100 MΩ and results together with a typical gate-to-source capacitance C_{gs} in a high-pass corner frequency of a few 100 Hz. Calculations carried out in Subsection 2.1.6 show a rough estimation for the corner frequency f_c on the order of 242.466 Hz for the Knowles Acoustics MD9745APA-1 microphone.

2.1.5 Interfacing the Electret Microphone

The metallized electret foil diaphragm is contacted through a metal contact ring to the microphone capsule and connected to the source of the JFET. The metal backplate is connected to the gate of the JFET. For the microphone of the type Knowles Acoustics MD9745APA-1, these facts are indicated in the data sheet [10]. A resistor can be switched in between the source of the JFET and ground to limit the bias current of the JFET. However, Kurt Heutschi, lecturer for acoustics at ETH, pointed out that the membrane does not need to be directly connected to the source of the JFET and that other JFET buffer principles exist in literature. For instance, [3] uses a microphone model with a JFET in a common-drain configuration and a source resistor of $R_s = 20$ kΩ to buffer the gate voltage.

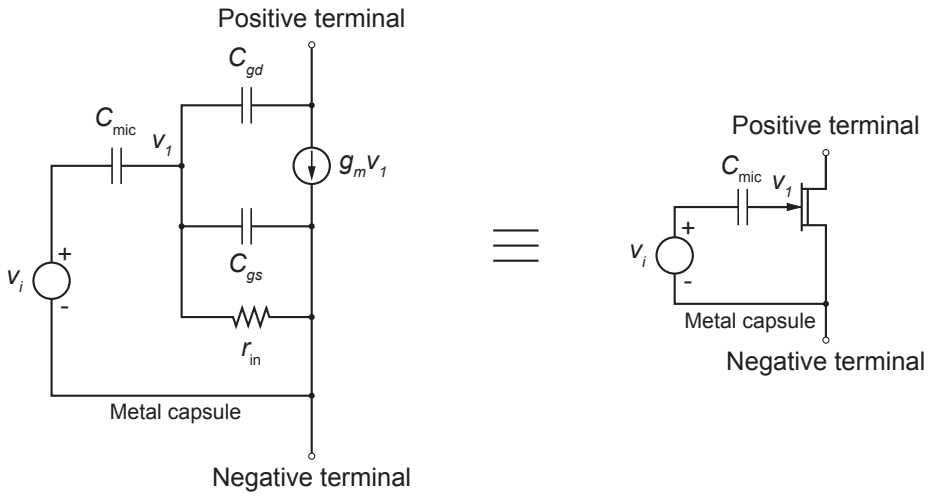


Figure 2.5: Microphone model used for simulations with T-SPICE. Circuit parameters: $C_{\text{mic}} = 1$ nF, $C_{gs} = 220$ pF, $C_{gd} = 160$ pF, $r_{\text{in}} = 100$ MΩ.

2.1.6 Numerical Calculations

An electret microphone of the type Knowles Acoustics MD9745APA-1 was opened to calculate the microphone capacitance C_{mic}. The outer diameter d_1, the width w and the thickness t of the spacer (see Fig. 2.1) were measured with a micrometer and are listed in Table 2.1. The spacer reduces the effective diameter of the diaphragm

$$d_2 = d_1 - 2 \cdot w \tag{2.4}$$

The effective diaphragm area is given by

$$A = \left(\frac{d_2}{2}\right)^2 \cdot \pi = 37.068 \text{ mm}^2 \tag{2.5}$$

$$C_{\text{mic}} = \frac{\varepsilon_0 \varepsilon_r A}{t} = \frac{8.854 \times 10^{-12} \frac{\text{F}}{\text{m}} \cdot \left(\frac{6.87 \times 10^{-3} \text{ m}}{2}\right)^2 \cdot \pi}{50 \times 10^{-6} \text{ m}} = 6.564 \text{ pF} \tag{2.6}$$

where $\varepsilon_0 = 8.854 \cdot 10^{-12}$ F/m is the dielectric constant and $\varepsilon_r = 1$ the relative dielectric constant of air. The corner frequency of the high-pass filter is estimated to be

$$f_c = \frac{1}{2\pi \cdot r_{\text{in}} C_{\text{mic}}} = \frac{1}{2\pi \cdot 100 \times 10^6 \,\Omega \cdot 6.564 \times 10^{-12} \,\text{F}} = 242.466 \text{ Hz} \tag{2.7}$$

This result of f_c is in good accordance with the values in literature on the order of 100 Hz.

d_1	8.87 mm
w	1 mm
d_2	6.87 mm
d	8 mm
t	50 μm
C_{mic}	6.564 pF
f_c	242.466 Hz

Table 2.1: Measured dimensions and circuit parameters of the microphone (Knowles Acoustics MD9745APA-1).

Part	Producer	Number
Operational amplifier	National Semiconductor	LMC6484IN
N-type JFET	Fairchild Semiconductor	BF244A/B
P-type MOSFET	Vishay Siliconix	BS250
Electret microphone	Knowles Acoustics	MD9745APA-1

Table 2.2: Discrete components used for the experiments on the proto board.

2.2 Experiments

The main results arising from experiments with the electret microphone, the JFET and the microphone preamplifier as described in [3] are presented. A microphone of the type Knowles Acoustics MD9745APA-1 was used for the experiments (see Table 2.2). Its typical sensitivity is -41 dB which corresponds to 8.913 mV/Pa (note that 0 dB = 1 V/Pa) [10].

2.2.1 Electret Microphone

In the first experiment, resistors R_s of different values were connected between the negative terminal of the microphone and ground and the bias currents were measured. The plots are shown in Fig. 2.6. Qualitatively, the source resistor causes a voltage drop which in turn reduces the effective drain-to-source voltage V_{ds} of the JFET and thus the bias current of the microphone.

It turns out that the linear (or triode) region of the JFET is further extended for higher drain-to-source voltages, which means that for the same drain-to-source voltage the JFET is made to operate in the linear region when a source resistor is added. In this way the bias current of the microphone is drastically reduced and more linearity is achieved. It is important to note that switching in a source resistor has no effect on the gate-to-source voltage V_{gs} of the JFET.

Access to internal nodes of the microphone was not possible because charge on the gate of the JFET would leak away and noise might be coupled into the high-

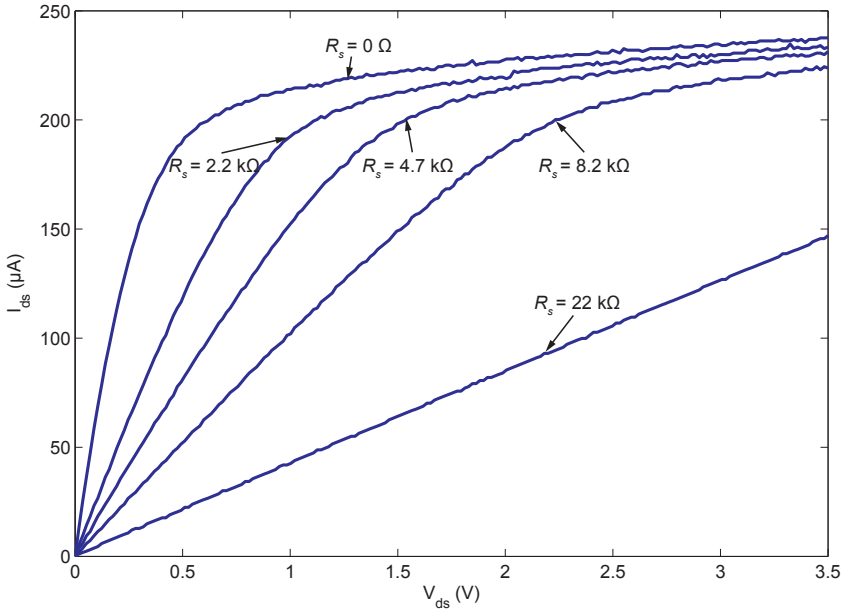


Figure 2.6: Plot of the microphone currents for different source resistors as a function of the voltage between the microphone terminals. A comparison between the curves shows that the linearity in the triode region is increased with higher source resistors.

impedance node. Also, the small-signal parameters of the JFET, like parasitic gate-to-source C_{gs} and gate-to-drain C_{gd} capacitance could not easily be characterized.

2.2.2 Microphone Preamplifier

A setup of the microphone preamplifier proposed in [3] was built of discrete circuit elements (see Table 2.2) on a proto board. Refer to Fig. 3.2 in Chapter 3 for a schematic of the circuit. The OTA for adaptation was replaced with an OpAmp and a high resistor in the order of 1 MΩ in series with the OpAmp output. The amplification and the DC adaptation mechanism could be experimentally verified. However, it is not sure how reliable the results are because only high-voltage MOSFETs were provided.

A slightly different value for the transconductance parameter β resulted from the experiments and was incorporated into the nJFET model in T-Spice. β was doubled and now is equal to 6×10^{-5} A/V^2.

2.3 Preamplifier with Controllable Feedback Resistor

In the context of a binaural silicon cochlea chip designed by Shih-Chii Liu, we also designed and laid out a microphone preamplifier based on [3], which uses a

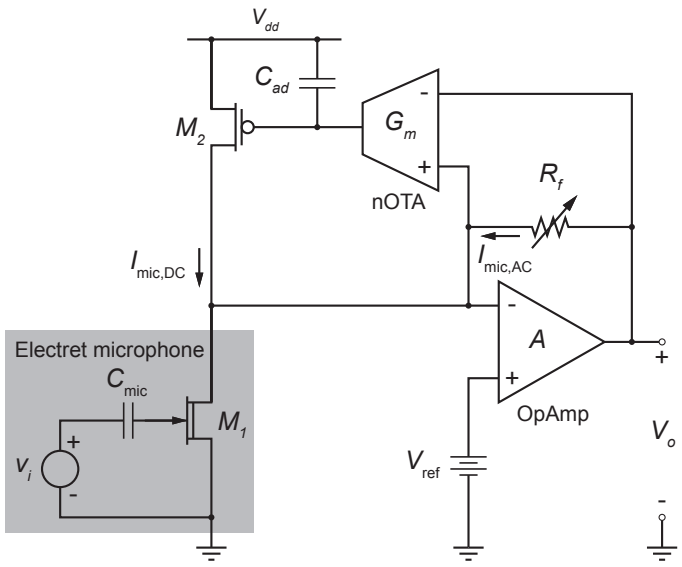


Figure 2.7: Schematic of the microphone preamplifier with controllable feedback resistor.

controllable feedback resistor. The schematic of the circuit is shown in Fig. 2.7. The working principle of the microphone preamplifier is discussed in Section 3.1 of Chapter 3 in detail. Since electret microphones come in a great variety with cheap and expensive types differing in their sensitivity, it was desirable to implement a microphone preamplifier with a variable feedback resistor, and thus variable gain to adjust the amplitude of the AC voltage at the output. A sketch of the variable resistor is shown in Fig. 2.8.

The control logic was implemented according to the truth table in Table 2.3.

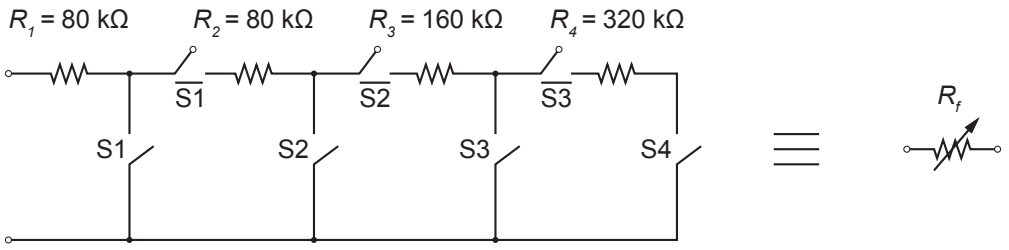


Figure 2.8: Schematic of the controllable resistor. S1 closed corresponds to 80 kΩ, S2 closed corresponds to a total 160 kΩ, S3 closed corresponds to a total 320 kΩ, S4 closed corresponds to a total 640 kΩ.

Switches				Control signals	
80 kΩ S1	80 kΩ S2	160 kΩ S3	320 kΩ S4	C1	C2
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

Table 2.3: Truth table of the control logic for the controllable resistor.

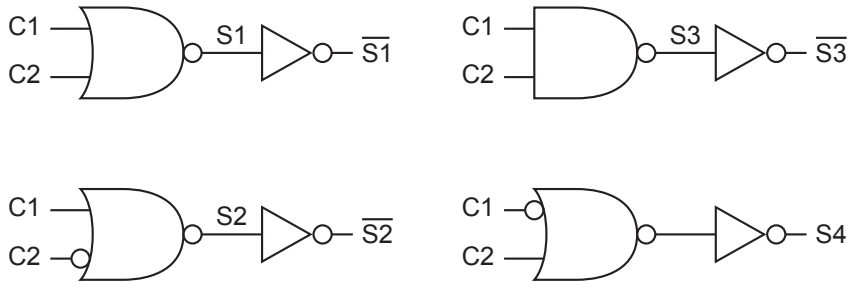


Figure 2.9: Gate implementation of the control logic for the controllable resistor.

The logic equations are as follows

$$S1 = \overline{C1} \wedge \overline{C2} = \overline{C1 \vee C2} \tag{2.8}$$

$$S2 = \overline{C1} \wedge C2 = \overline{C1 \vee \overline{C2}} \tag{2.9}$$

$$S3 = C1 \wedge \overline{C2} = \overline{\overline{C1} \vee C2} \tag{2.10}$$

$$S4 = C1 \wedge C2 = \overline{\overline{C1} \wedge \overline{C2}} \tag{2.11}$$

Refer to Fig. 2.9 for an overview of the gate implementation of the control logic. NAND and NOR gates were used along with inverters exclusively. The schematics of the logic gates are depicted in Fig. 2.10.

Minimum transistor sizes were used for the logic transistors. The switches to switch in the different resistor legs were implemented as wide transmission gates (T-gates) for low on-resistance. Two complementary switches were used for each resistor leg to both switch in the resistor leg and to disable the parasitic effects of the other legs because a parasitic capacitance is associated with each resistor. It is apparent that resistor values of 80 kΩ, 160 kΩ, 320 kΩ and 640 kΩ can be realized.

Two preamplifiers were placed on the chip, one for each ear (left and right channel). The control logic could be shared because the feedback resistor has the the same value for both the left and the right channel. A Bode plot of the various

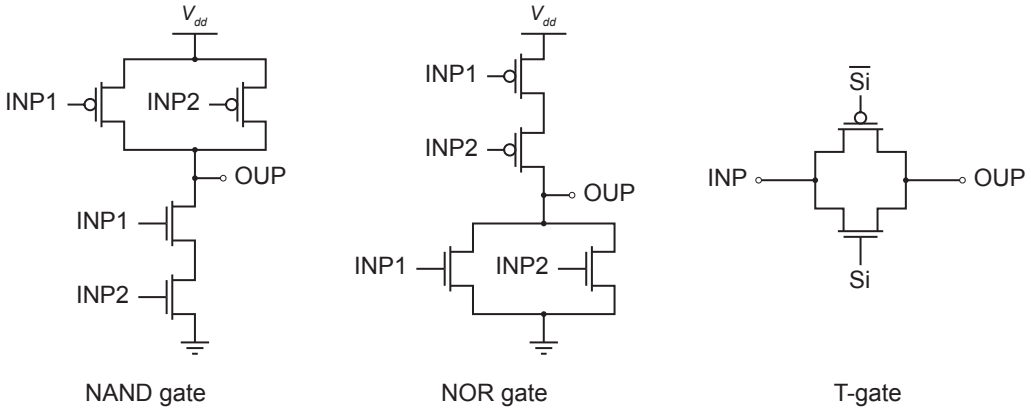


Figure 2.10: Logic gates used in the control logic.

transfer functions for different values of the feedback resistor R_s with $C_{ad} = 6$ pF and $R_s = 0\ \Omega$ is shown in Fig. 2.11.

Fabrication will be done in the MOSIS 0.35 μm CMOS process where four metal and two poly silicon layers are available. The designed layout is shown in Fig. 2.12.

2.4 Novel Approaches for Low-Power Audio Amplifiers

The requirements for a microphone preamplifier can be summarized as follows:

- The drain-to-source voltage V_{ds} of the JFET and the output voltage of the preamplifier must be decoupled, i.e. both the voltage across the JFET and the DC level of the output voltage of the preamplifier can be set independently.
- High power-supply rejection ratio (PSRR) because the device will be battery powered and devices such as motors can cause large transient supply drops.
- Low power consumption.
- Wide dynamic range.
- Current-mode adaptation with an adaptive element to separate the DC and AC components of the microphone current.
- Non-custom design, i.e. every electret microphone can be used.
- Amplification of the signal across a resistor for current-to-voltage conversion. An active circuit element in a feedback configuration is required for the amplification.
- A stable operating point has to be reached after power-up within a fraction of a second.

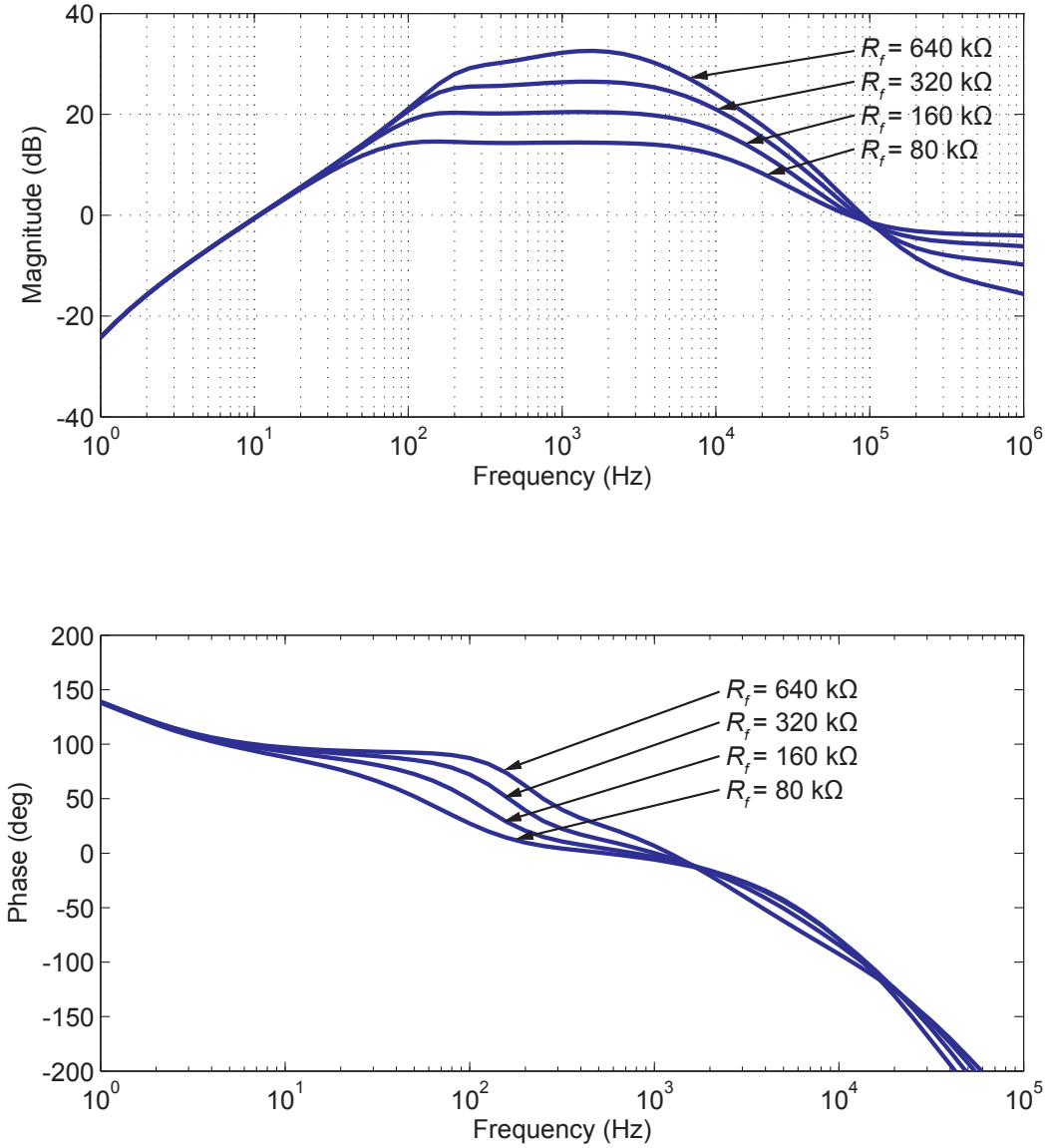


Figure 2.11: Bode plot of the transfer function of the preamplifier with controllable feedback resistor showing the gain and phase from the equivalent microphone AC signal voltage source to the preamplifier output. Circuit parameters: $C_{ad} = 6$ pF, $R_s = 0\ \Omega$, $I_{\mathrm{b1,OA}} = 30$ nA, $I_{\mathrm{b2,OA}} = 1\ \mu$A, $I_{\mathrm{b,OTA}} = 1$ pA.

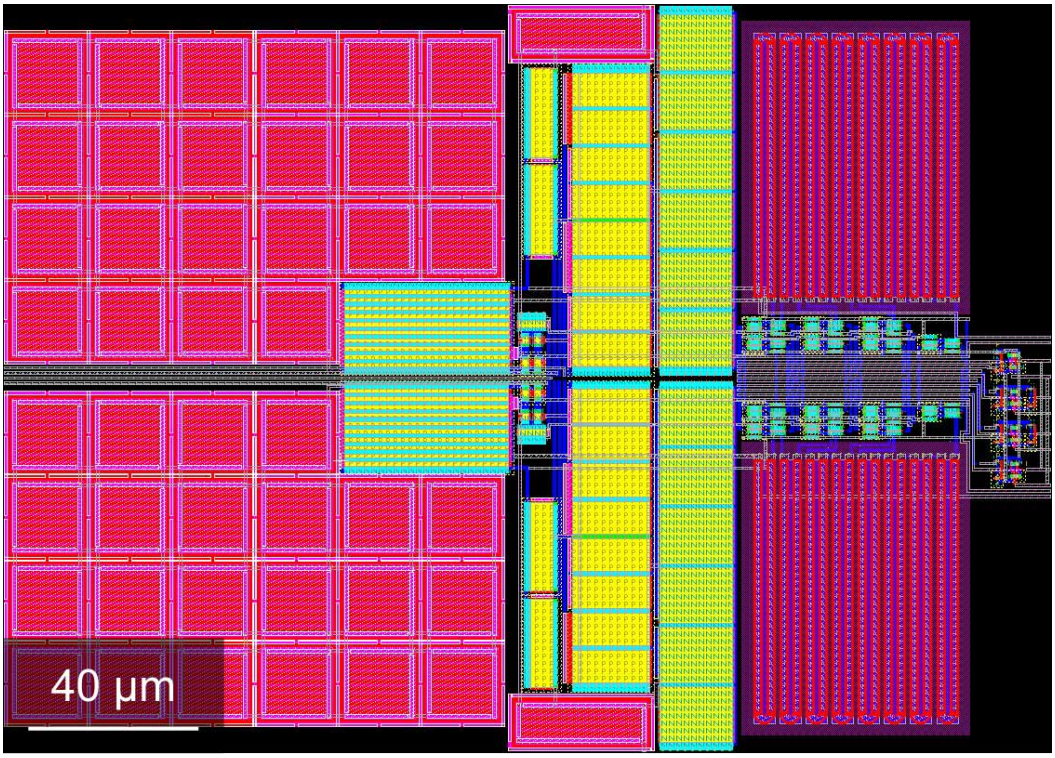


Figure 2.12: Chip layout.

2.4.1 Architecture of the Microphone Preamplifier

Conventional microphone preamplifiers like [3] operate with a huge microphone bias current in the order of 220 μA at a 3.3 V power supply and consume too much power. A way to trade signal-to-noise ratio (SNR) versus power in the microphone preamplifier based on [3] is to dynamically control a resistor between the negative terminal of the microphone and ground. Because sound and speech correlate, it is conceivable to switch between two modes differing in the source resistance: An ultra low-power mode (huge source resistor) with reduced bias current and sensitivity which is capable of detecting sound and a normal low-power mode (ordinary source resistor) with standard circuit operation which amplifies the microphone signal for speech processing.

Circuit operation after power-up starts in the ultra low-power mode. As soon as sound is detected, the circuit switches to the high-sensitivity mode which is appropriate to detect speech. After a time-out that is set by a leakage transistor in the sound detector, the high-sensitivity mode is left and the microphone preamplifier returns into the low-sensitivity mode. Fig. 2.13 illustrates the basic architecture of the microphone preamplifier including the sound detector.

2.4.2 Sound Detector

An OpAmp in the sound detector first compares the voltage at the microphone preamplifier output V_{in} with a threshold voltage V_{th} (see Fig. 2.14). If the signal voltage exceeds the threshold voltage, the capacitor C is charged through the diode-connected transistor M_1 which is forward biased. Note that capacitor C cannot be discharged through M_1. The capacitor voltage V_C is shifted by the source follower, consisting of transistors M_3 and M_4. Once the capacitor voltage reaches a certain level the first inverter switches to the complementary state. Two more inverters follow to make steeper edges and in order to generate the signals `Ctrl` and $\overline{\texttt{Ctrl}}$ to control the transmission gates (T-gates) which in turn switch in resistor R_1 or R_2.

A time-out function is implemented by continuously discharging capacitor C through the leakage transistor M_2. When the capacitor voltage V_C falls below a certain level, the first inverter switches back to the complementary state. The inverters are implemented as starved inverters because otherwise the newly conserved power is wasted due to high switching currents.

Even when the microphone preamplifier operates in the ordinary low-power mode, it takes the circuit after power-up on the order of three seconds to settle to the DC operating point. Each time sound is detected in the ultra low-power mode and the circuit switches to the high-sensitivity mode, however, it takes the adaptive element a couple of seconds to adapt to the new microphone bias current because the capacitor C_{ad} has to be charged by the low-transconductance nOTA. This problem has not been resolved yet. A workaround may consist of also switching in a higher bias current source in the OTA.

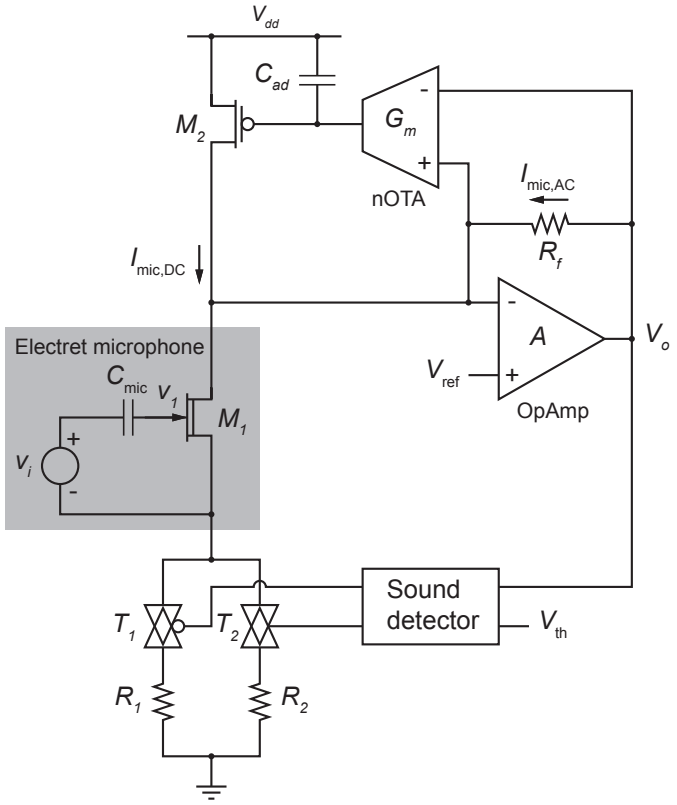


Figure 2.13: Schematic of the microphone preamplifier including the sound detector.

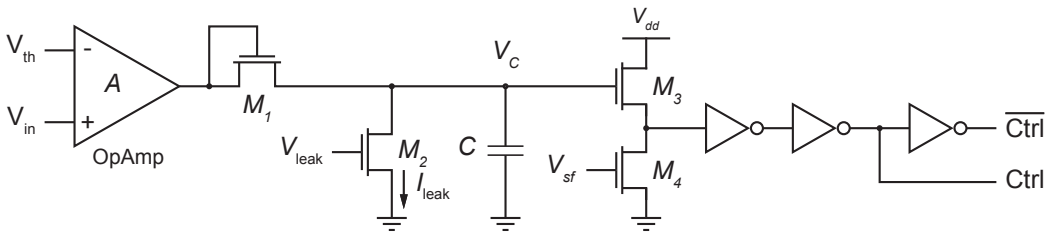


Figure 2.14: Possible implementation of the sound detector.

Chapter 3

Design of the Speech Detector

In this chapter we discuss the implementation of the speech detector with subthreshold analog circuits. The design aims at the MOSIS 1.6 μm process with a power supply of $V_{dd} = 3.3$ V. It should not use more area than a half of a MOSIS TinyChip (2.2×2.2 mm^2) because a face detection sensor will also be placed on the chip. The key figure of merit is the power consumption. The chip should be powered with an AA battery for about a year. The design must interface a microphone at the input and provide a digital output to a microcontroller. It must be able to bias itself without external components on the board. The order of the sections follows the signal processing from the input to the output (see Fig. 3.1). An overview of the signal processing algorithm is given in Section 1.5 in Chapter 1. Finally, the bias generator is addressed before concluding with the results of the chip-level simulation of the full speech detection circuit.

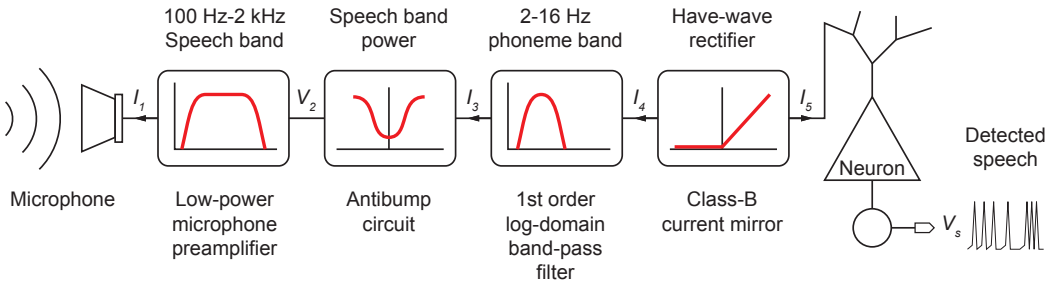


Figure 3.1: Circuit architecture of the speech detector showing the individual building blocks. The arrows at the interface of two blocks indicate whether it is a voltage or current input/output.

3.1 Microphone Preamplifier

The preamplifier chosen for implementation (see Fig. 3.2) is based on Baker and Sarpeshkar's circuit [3] which shows advantages in power-supply rejection ratio (PSRR), a high gain and a relatively low power consumption. It separates the DC and AC components of the microphone current and converts the small-signal current into a voltage across the feedback resistor.

Fig. 3.2 shows a schematic of the microphone preamplifier. The design contains a low-frequency feedback loop to adapt to the DC bias current $I_{\text{mic,DC}}$ of the microphone. The DC bias current is sensed by the adaptive element and sourced by the pFET, M_2, whereas the AC current $I_{\text{mic,AC}}$ is fed through the feedback resistor R_f. The AC current is sensed with a sense-amplifier configuration and converted into an AC voltage across the feedback resistor with the DC voltage component determined by the reference voltage at the non-inverting input of the OpAmp. Intuitively, subtracting the DC component of the total signal, combined with the finite bandwidth of the circuit leads to a transfer characteristic with the shape of a band-pass filter.

3.1.1 Operational Amplifier (OpAmp)

The p-type OpAmp is implemented as a simple Miller OpAmp. It should be capable of driving off-chip loads in the order of 1 pF or even more. The cutoff frequency can be changed by varying the Miller capacitor C_M. A higher C_M moves the dominant pole to lower frequencies. In this design, a Miller capacitor of $C_M = 300$ fF was chosen.

A large transistor length L in the OpAmp input stage improves matching and makes a high Early voltage for high gain. The aspect ratios of the transistors in the OpAmp were directly taken from the OpAmp presented in [3].

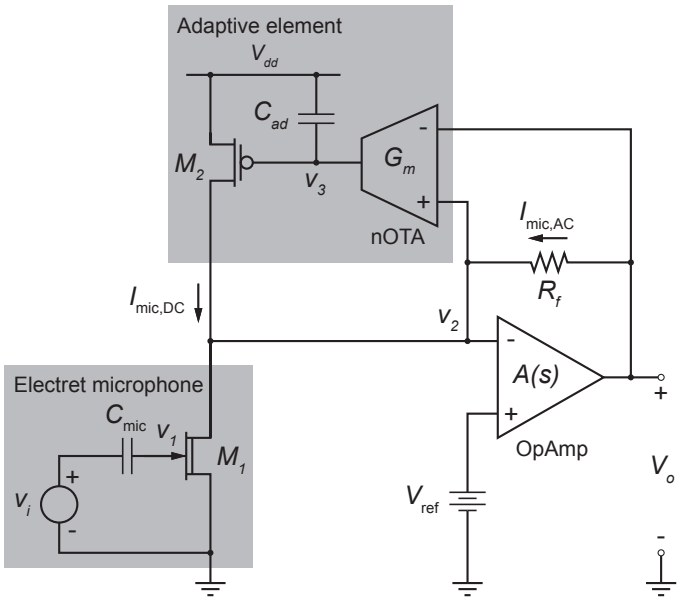
The OpAmp was simulated in a feedback configuration with a feedback resistor of 1 GΩ between the output and the inverting input and a load capacitor of $C_L = 2$ pF to explore pseudo-open loop characteristics. This configuration results in a extremely high time constant of the feedback path. The inverting input was coupled to ground through a 1 F capacitor. The DC voltage at the non-inverting input was 1.3 V. The simulation results are illustrated in the Bode plot of Fig. 3.3.

A cutoff frequency of $f_{\text{p,OA}} = 400$ mHz and a DC voltage gain of $A_{\text{DC,OA}} = 116.68$ dB were found. We assume that the gain function $A(s)$ of the operational amplifier contains a single pole

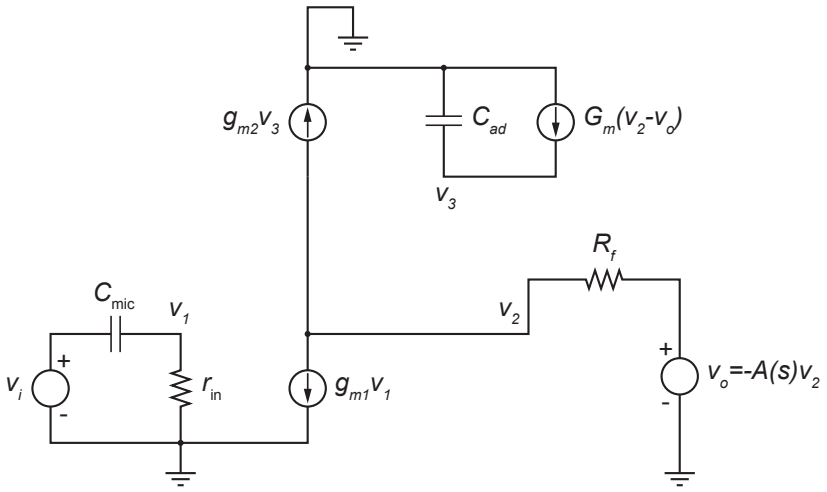
$$A(s) = \frac{A_{\text{DC,OA}}}{1 - \frac{s}{p_{\text{OA}}}} = \frac{A_{\text{DC,OA}}}{1 + s \cdot \tau_{\text{p,OA}}} \tag{3.1}$$

where $A_{\text{DC,OA}}$ is the low-frequency gain and $\tau_{\text{p,OA}}$ is the time constant of the pole of the OpAmp. The gain-bandwidth product of the OpAmp is given by

$$\text{GBP}_{\text{OA}} = A_{\text{DC,OA}} \cdot |p_{\text{OA}}| = A_{\text{DC,OA}} \cdot 2\pi f_{\text{OA}} = 1.7149 \text{ MHz} \tag{3.2}$$



(a)



(b)

Figure 3.2: (a) Circuit topology of the microphone preamplifier including a p-type OpAmp, an n-type OTA and an adaptive element. Note that a resistance R_s can be switched in between the source of the JFET and ground to reduce the bias current of the JFET and thus the power consumption. (b) Small-signal equivalent circuit as used for the derivation of the transfer function of the microphone preamplifier.

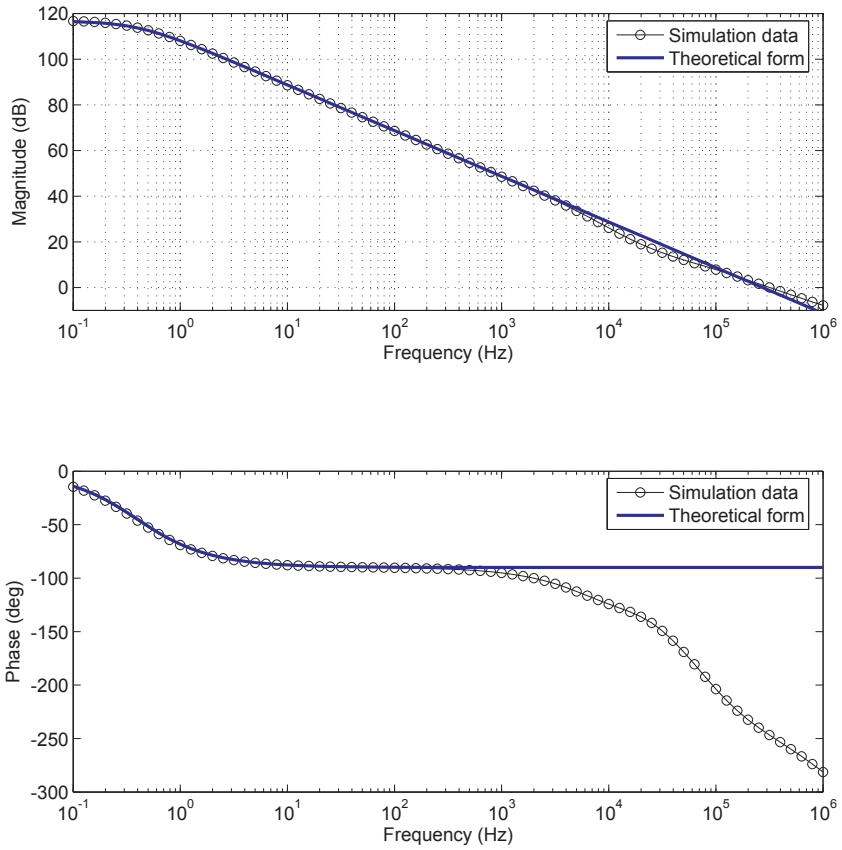


Figure 3.3: Gain magnitude and phase versus frequency for the operational amplifier (OpAmp). The simulation shows that the assumption of a dominant pole at low frequencies and the approximation of the gain function below 1 kHz are valid.

For proper large-signal behavior it is important that the output stage of the Miller OpAmp can provide at least the AC signal current of the microphone. Otherwise, the differential input voltage cannot be balanced to be zero and the OpAmp starts to slew causing clipping of the AC signal.

3.1.2 Operational Transconductance Amplifier (OTA)

A simple 5-transistor low-current n-type OTA (nOTA) with an aspect ratio of $W/L = 6\lambda/24\lambda$ was chosen for implementation. A large transistor length L increases the gain because it effects in a higher output resistance. As another benefit, transistor mismatch has less influence on the circuit behavior. The OTA is a differential to single-ended transconductor and determines in the context of the adaptive element the pass-band in the transfer function of the microphone preamplifier.

3.1.3 Adaptive Element

The capacitor for adaptation is equal to $C_{ad} = 10$ pF. AC analysis and detailed calculations of the transfer function of the preamplifier in Appendix A have shown that the pFET of the adaptive element, M_2, affects the cutoff frequency of the band-pass characteristic. A wide and short transistor was chosen to set the cutoff frequency around 2 kHz. As a side effect, the parasitic capacitances C_{gs} and C_{gb} of M_2 increase the effective capacitance $C_{\text{ad,tot}}$ of the adaptive element. Therefore, the total capacitance contributing to the adaptation is given by

$$C_{\text{ad,tot}} = C_{ad} + C_{gs2} + C_{gb2} = 11.225 \text{ pF} \tag{3.3}$$

3.1.4 Simplified Analysis of the Transfer Function

Here we analyze the small-signal transfer function of the microphone preamplifier from the equivalent microphone input voltage source v_i to the preamplifier output v_o. Second-order effects, such as channel-length modulation (or Early effect), which leads to finite output resistance, and parasistic node capacitance, are neglected. Furthermore, the impedance between the source of the microphone JFET and ground is not considered. The small-signal equivalent circuit is depicted in Fig. 3.2.

Since C_{mic} and r_{in} form a voltage divider across v_i, the gate-to-source voltage of the JFET is given by

$$v_1 = v_i \cdot \frac{r_{\text{in}}}{\frac{1}{sC_{\text{mic}}} + r_{\text{in}}} \tag{3.4}$$

The output voltage of the OpAmp is

$$v_o = -A(s) \cdot v_2 \tag{3.5}$$

where $A(s)$ is the gain of the OpAmp open-loop transfer function. Assuming that the OpAmp has a dominant pole, from Eq. (3.1) the OpAmp transfer function (or gain) is

$$A(s) = \frac{A_{\mathrm{DC,OA}}}{1 + s \cdot \tau_{\mathrm{p,OA}}} \tag{3.6}$$

where $A_{\mathrm{DC,OA}}$ is the low-frequency voltage gain and $\tau_{\mathrm{p,OA}}$ is the time constant of the pole of the OpAmp. From Kirchhoff's current law (KCL) at node v_2

$$-g_{m1}v_1 - g_{m2}v_3 - \frac{1 + A(s)}{R_f}v_2 = 0 \tag{3.7}$$

Kirchhoff's voltage law (KVL) at node v_3 gives

$$v_3 = G_m(v_2 - v_o) \cdot \frac{1}{sC_{ad}} \tag{3.8}$$

Solving Eq. (3.5) for $v_2 = -v_0/A(s)$, substituting it together with Eq. (3.8) into Eq. (3.7) gives

$$-\frac{g_{m1}r_{\mathrm{in}}}{\frac{1}{sC_{\mathrm{mic}}} + r_{\mathrm{in}}}v_i + \frac{G_m g_{m2}\left(1 + \frac{1}{A(s)}\right)}{sC_{ad}}v_o + \frac{1 + \frac{1}{A(s)}}{R_f}v_o = 0 \tag{3.9}$$

The transfer function from the equivalent microphone AC signal voltage source v_i to the preamplifier output v_o is given by

$$H(s) = \frac{v_0}{v_i} = \frac{\frac{g_{m1}r_{\mathrm{in}}}{\frac{1}{sC_{\mathrm{mic}}} + r_{\mathrm{in}}}}{\frac{G_m g_{m2}\left(1 + \frac{1}{A(s)}\right)}{sC_{ad}} + \frac{1 + \frac{1}{A(s)}}{R_f}} \tag{3.10}$$

Rearranging and multiplying nominator and denominator by R_f/r_{in} gives

$$H(s) = \frac{g_{m1}R_f}{\left(\frac{G_m g_{m2}R_f}{sC_{ad}} + 1\right)\left(\frac{1}{sC_{\mathrm{mic}}r_{\mathrm{in}}} + 1\right)\left(1 + \frac{1}{A(s)}\right)} \tag{3.11}$$

Substituting the gain of the OpAmp A from Eq. (3.6) into the previous equation yields

$$H(s) = \frac{g_{m1}R_f}{\left(\frac{G_m g_{m2}R_f}{sC_{ad}} + 1\right)\left(\frac{1}{sC_{\mathrm{mic}}r_{\mathrm{in}}} + 1\right)\left(1 + \frac{1 + s\tau_{\mathrm{p,OA}}}{A_{\mathrm{DC,OA}}}\right)} \tag{3.12}$$

The term $(1 + 1/A(s))$ can be rewritten as

$$1 + \frac{1}{A(s)} = \frac{A_{\mathrm{DC,OA}} + 1 + s\tau_{\mathrm{p,OA}}}{A_{\mathrm{DC,OA}}} = \frac{A_{\mathrm{DC,OA}} + 1}{A_{\mathrm{DC,OA}}}\left(1 + s\frac{\tau_{\mathrm{p,OA}}}{A_{\mathrm{DC,OA}} + 1}\right) \tag{3.13}$$

Hence, the transfer function from Eq. (3.12) simplifies to

$$H(s) = \frac{g_{m1}R_f \frac{A_{\mathrm{DC,OA}}}{A_{\mathrm{DC,OA}}+1}}{\left(\frac{G_m g_{m2} R_f}{sC_{ad}} + 1\right)\left(\frac{1}{sC_{\mathrm{mic}}r_{\mathrm{in}}} + 1\right)\left(1 + s\frac{\tau_{\mathrm{p,OA}}}{A_{\mathrm{DC,OA}}+1}\right)} \tag{3.14}$$

$$= \frac{H_{\mathrm{PB}}}{\left(\frac{1}{s\tau_{p1}} + 1\right)\left(\frac{1}{s\tau_{p2}} + 1\right)(1 + s\tau_{p3})} \tag{3.15}$$

where

$$H_{\mathrm{PB}} = g_{m1}R_f \frac{A_{\mathrm{DC,OA}}}{A_{\mathrm{DC,OA}} + 1} \tag{3.16}$$

$$\tau_{p1} = C_{\mathrm{mic}}r_{\mathrm{in}} \tag{3.17}$$

$$\tau_{p2} = \frac{C_{ad}}{G_m g_{m2} R_f} \tag{3.18}$$

$$\tau_{p3} = \frac{\tau_{\mathrm{p,OA}}}{A_{\mathrm{DC,OA}} + 1} \tag{3.19}$$

$H(s)$ is the transfer function from the equivalent microphone AC signal voltage source v_i to the preamplifier output v_o. H_{PB} is the voltage gain in the pass-band (or in-band voltage gain). It is obvious that τ_{p1} corresponds to the pole at low frequencies caused by the electret microphone capacitor C_{mic} and the huge input resistance r_{in} of the JFET as discussed in Subsection 2.1.4 of Chapter 2. The second pole τ_{p2} is due to the presence of the adaptive element, formed by the capacitor C_{ad} and the transconductance G_m of the nOTA. Because of the feedback configuration, the pole of the OpAmp τ_{p3} is moved to much higher frequencies. That is not a surprise because gain is traded for bandwidth.

However, the foregoing analysis is not accurate as far as the high-frequency behavior of the circuit (i.e. the pole causing the rolloff) is concerned. It is shown in Appendix A that the bandwidth limiting factor is mainly capacitive coupling through the gate-to-drain capacitance C_{gd2} of the pFET, M_2, of the adaptive element. As a consequence, a small-signal current is generated by g_{m2} which causes a finite resistance, looking into the pFET. The equivalent resistance R_{eq} forms in conjunction with the feedback resistor R_f a voltage divider across the OpAmp which decreases the fraction of the voltage from the output of the OpAmp that is fed back to the inverting input of the OpAmp. This effect substantially reduces the bandwidth of the circuit. Thus, the pole causing the rolloff is given by

$$p_3 = -\frac{A_{\mathrm{DC,OA}}(C_{\mathrm{ad,tot}} + C_{gd2})}{\tau_{\mathrm{p,OA}} C_{gd2} g_{m2} R_f} = -\frac{\mathrm{GBP_{OA}}(C_{\mathrm{ad,tot}} + C_{gd2})}{C_{gd2} g_{m2} R_f} \tag{3.20}$$

where $C_{\mathrm{ad,tot}}$ is the effective capacitance of the adaptive element and $\mathrm{GBP_{OA}}$ is the gain-bandwidth product of the OpAmp. The simulation parameters can be found in Table 3.1. The simulations were done with a microphone model provided by Michael Baker, one of the authors of [3], including a microphone capacitor of $C_{\mathrm{mic}} = 1$ nF.

OpAmp
$I_{\mathrm{b1,OA}} = 46.8$ nA
$I_{\mathrm{b2,OA}} = 11\ \mu$A
$C_M = 300$ fF
$A_{\mathrm{DC,OA}} = 116.68$ dB
$f_{\mathrm{p,OA}} = 400$ mHz
$\mathrm{GBP_{OA}} = 1.7149$ MHz
$V_{\mathrm{ref}} = 1.3$ V
OTA
$I_{\mathrm{b,OTA}} = 7.69$ pA
$\kappa = 0.7$
$G_m = 105.96$ pS
$R_o = 9.0416 \times 10^{12}\ \Omega$

JFET
$g_{m1} = 247\mu$S
$g_{ds1} = 15\mu$S
$C_{gs1} = 220$ pF
$C_{gs1} = 160$ pF
pFET
$g_{m2} = 1.24$ mS
$g_{ds2} = 3\mu$S
$C_{gs2} = 415$ fF
$C_{gd2} = 6.57$ pF
$C_{gb2} = 810$ fF

$C_{\mathrm{mic}} = 1$ nF
$r_{\mathrm{in}} = 100$ MΩ
$R_f = 300$ kΩ
$C_{ad} = 10$ pF
$C_{\mathrm{ad,tot}} = 11.225$ pF

Table 3.1: (Small-signal) circuit parameters of the microphone preamplifier extracted from T-Spice.

3.1.5 Numerical Calculations

Fig. 3.4 shows the Bode plot of the transfer characteristic of the microphone preamplifier obtained from AC simulations with T-Spice together with the plots of the analytically derived transfer functions. The small-signal parameters extracted from T-Spice were used for the calculation of the pass-band gain and the pole frequencies of the analytical expression (see Table 3.1). Evaluation of Eqs. (3.16) to (3.19) gives

$$H_{\mathrm{PB}} = g_{m1} R_f \frac{A_{\mathrm{DC,OA}}}{A_{\mathrm{DC,OA}} + 1} = 37.3964 \text{ dB} \tag{3.21}$$

$$f_{p1} = \frac{1}{2\pi\tau_{p1}} = \frac{1}{2\pi C_{\mathrm{mic}} r_{\mathrm{in}}} = 1.5915 \text{ Hz} \tag{3.22}$$

$$f_{p2} = \frac{1}{2\pi\tau_{p2}} = \frac{G_m g_{m2} R_f}{2\pi C_{ad}} = 627.3429 \text{ Hz} \tag{3.23}$$

$$f_{p3} = \frac{1}{2\pi\tau_{p3}} = \frac{1 + A_{\mathrm{DC,OA}}}{2\pi\tau_{\mathrm{p,OA}}} = 272.94 \text{ kHz} \tag{3.24}$$

H_{PB} is the pass-band gain of the preamplifier, f_{p1} is the frequency of the first pole caused by the microphone, f_{p2} is the frequency of the second pole caused by the adaptive element and f_{p3} is the frequency of the pole due to the finite bandwidth of the OpAmp. It can be seen that the calculations of the low-frequency poles are in good agreement with those derived from the simulation data. Note that second-order effects such as channel-length modulation and parasitic capacitance have not been considered.

A more elaborate analysis of the microphone preamplifier in Appendix A shows

that from Eq. (A.31) the pole frequency of the third pole is given by

$$f_{p3} = \frac{|p_3|}{2\pi} = \frac{A_{\mathrm{DC,OA}}(C_{\mathrm{ad,tot}} + C_{gd2})}{2\pi\tau_{\mathrm{p,OA}} C_{gd2} g_{m2} R_f} = 1.9872 \text{ kHz} \tag{3.25}$$

3.2 Squaring Circuit

The squaring circuit consists of an adaptive element to obtain the DC level of the input voltage and an antibump circuit [12] which performs the actual squaring operation. A circuit schematic of the squaring circuit is shown in Fig. 3.5.

3.2.1 Adaptive Element

The voltage of the speech signal at the preamplifier output has to be squared to determine the power of the signal. Because the differential input of the squaring circuit is squared, one input to the antibump circuit has to adapt to the DC level of the other input. Ideally, the DC level is equal to the reference voltage at the non-inverting input of the OpAmp, however, because of voltage offsets in the OpAmp and the OTA of the previous preamplifier stage, the DC level in the physical circuit might slightly differ from the ideal value. That is the reason why an adaptive element is required. The ideal adaptive element has a characteristic of a low-pass filter with a high time constant to cause a cutoff frequency at least below the lowest frequency of the speech band around 100 Hz.

The proposed adaptive element from [13] could not be used because the associated RC time constant was too long. It led to an excessive settling time of the circuit after power-up that cannot be tolerated. It was replaced with a simple follower integrator circuit consisting of an p-type OTA (pOTA) and a capacitor C. As described in [11] (p. 252), the equivalent transconductance is

$$G = \frac{\kappa I_b}{2U_T} \tag{3.26}$$

where κ is the subthreshold slope factor, I_b the bias current of the OTA and $U_T = kT/q = 25.4$ mV the thermal voltage. The time constant is given by

$$\tau = \frac{C}{G} \tag{3.27}$$

The cutoff frequency is equal to

$$f_c = \frac{1}{2\pi\tau} = \frac{G}{2\pi C} = \frac{\kappa I_b}{4\pi U_T C} \tag{3.28}$$

With $C = 1$ pF and $I_b = 1$ pA, this yields a cutoff frequency of $f_c = 140$ Hz. The cutoff frequency of the follower integrator has to be below 100 Hz in order to function as an adaptive element.

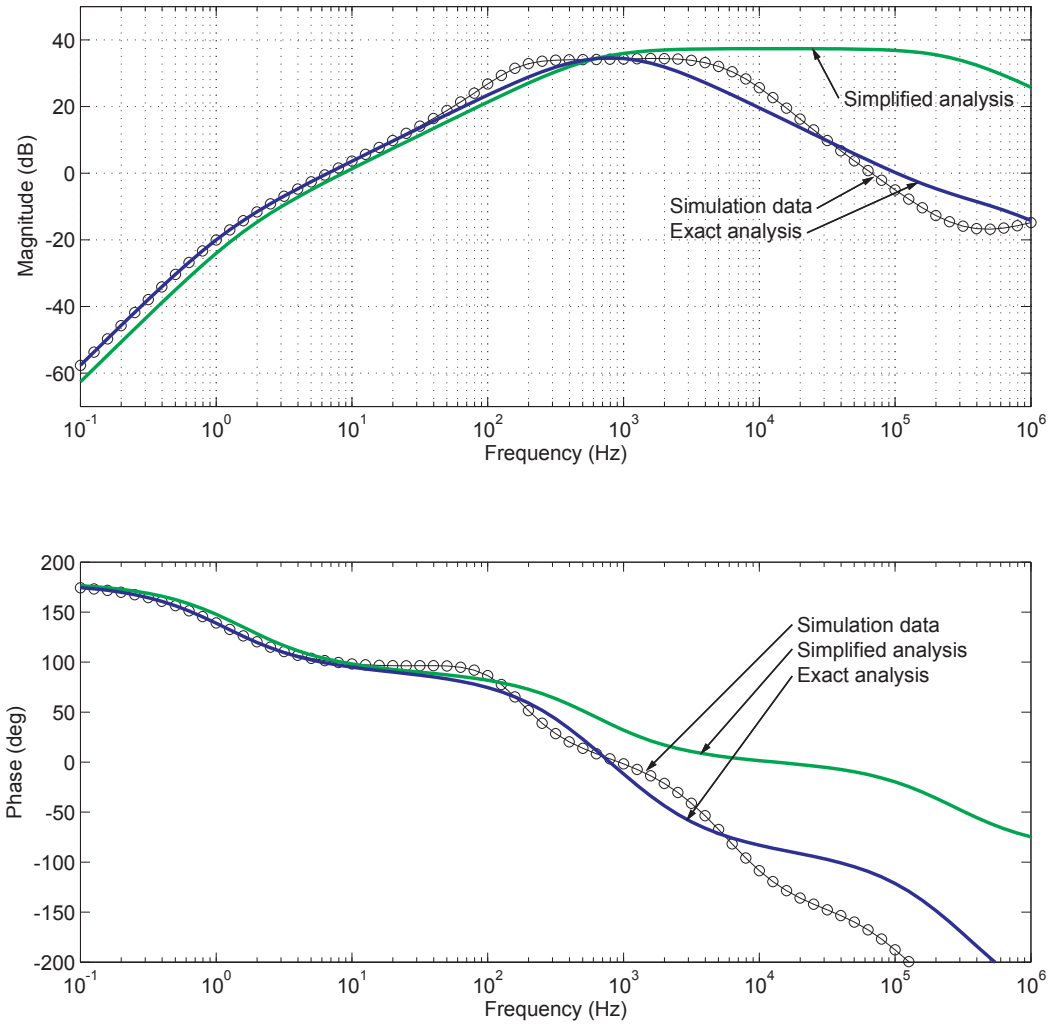


Figure 3.4: Bode plot of the simplified transfer function of the microphone preamplifier including the microphone model (without source resistor R_s). Data obtained from AC simulations with T-SPICE and from solving the set of equations of the simplified and the exact small-signal equivalent circuits is shown. The system of equations of the exact small-signal equivalent circuit (see Appendix A) was numerically solved with MATLAB.

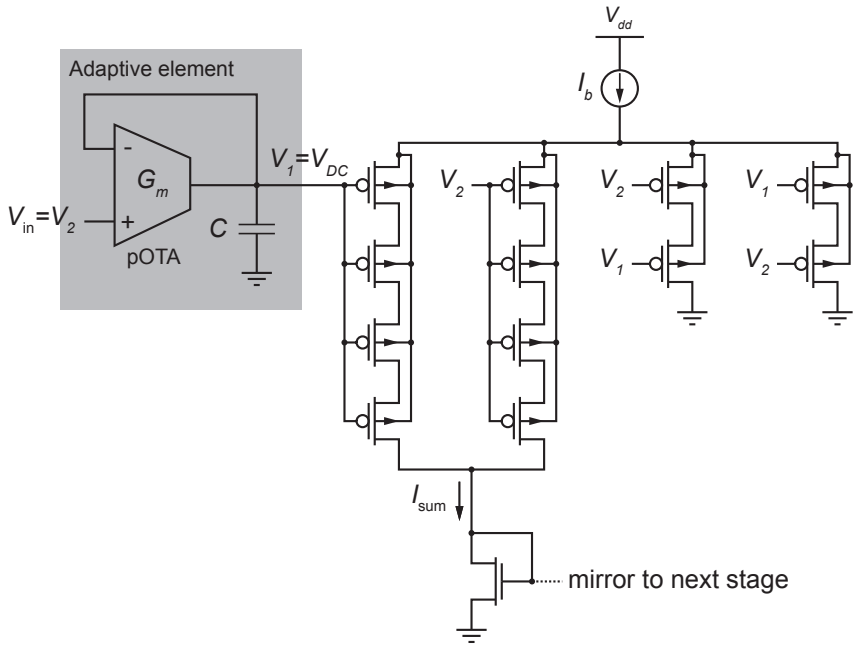


Figure 3.5: Schematic of the squaring circuit including the adaptive element. Circuit parameter: $C = 1$ pF.

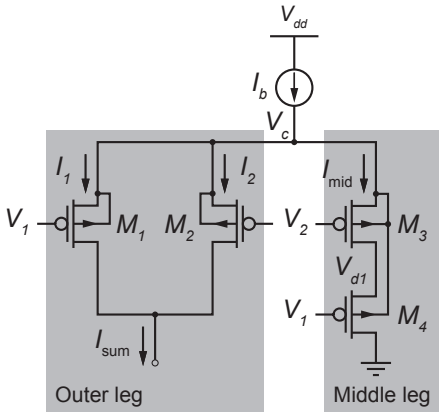


Figure 3.6: Schematic of the antibump circuit (simplified).

3.2.2 Antibump Circuit

A circuit capable of performing a squaring operation on the signal is needed to demodulate the speech signal back to the baseband and to compute its power. Antibump circuits as described in [12] are well-suited for that purpose because they feature an V–I input-to-output characteristic which is very similar to a parabola. In the following, the V–I characteristic is derived for a p-type antibump circuit.

The strength ratio is the ratio of the aspect ratio of the transistors in the middle leg, M_3 and M_4, to the aspect ratio in the outer legs, M_1 and M_2. This parameter is given by

$$S = \frac{(W/L)_{\text{middle}}}{(W/L)_{\text{outer}}} \tag{3.29}$$

and is used for the derivation of the circuit equations. In the analysis of the circuit, it is assumed for the sake of simplicity that the transistors in the outer legs are unit transistors and that the transistors in the middle leg are scaled by a factor S.

Fig. 3.6 shows the simplified antibump cicuit. It has three outputs: I_1, I_2 and I_{mid}. For the squaring function we are solely interested in the antibump output which is formed by combining the currents of the outer legs $I_{\text{sum}} = I_1 + I_2$. Qualitatively, we can understand the operation of the antibump circuit as follows: Due to Kirchhoff's current law (KCL), the three currents, I_1, I_2 and I_{mid}, must sum to the bias current I_b. Therefore, the voltage V_c follows the lower of V_1 or V_2.

As described in [11] (p. 170–175), current flows through all three legs of the circuit, if no differential voltage is applied $\Delta V = 0$. When $|\Delta V|$ increases, the common-node voltage V_c follows the lower of V_1 or V_2 and cuts off I_{mid}, because the transistor whose gate is connected to the higher of V_1 or V_2 shuts off. If both V_1 and V_2 fall together, I_{mid} does not increase, because the common-node voltage V_c decreases along with V_1 and V_2.

The general I–V equation for a pFET is [11] (p. 70)

$$I = I_0\, e^{\kappa(V_w - V_g)} \left(e^{-(V_w - V_s)} - e^{-(V_w - V_d)} \right) \tag{3.30}$$

where V_w is the bulk voltage of the MOSFET. To reduce common mode short and narrow channel effects, all pFET bulks are connected to their sources.

The transistors of the outer leg, M_1 and M_2, operate in the subthreshold saturation region. Hence, the currents I_1 and I_2 are given by[1]

$$I_1 = I_0\, e^{\kappa(V_c - V_1)}, \quad I_2 = I_0\, e^{\kappa(V_c - V_2)} \tag{3.31}$$

Transistors M_3 and M_4 of the middle leg work in the subthreshold triode and saturation region, respectively

$$I_3 = S \cdot I_0\, e^{\kappa(V_c - V_1)} \left(1 - e^{-(V_c - V_{d1})} \right) = S \cdot I_0 \left(e^{\kappa(V_c - V_1)} - e^{\kappa(V_c - V_1) - (V_c - V_{d1})} \right) \tag{3.32}$$

$$I_4 = S \cdot I_0\, e^{\kappa(V_c - V_2) - (V_c - V_{d1})} = S \cdot I_0\, e^{\kappa(V_c - V_2)} \cdot e^{-(V_c - V_{d1})} \tag{3.33}$$

Assuming that the currents through transistors M_3 and M_4 are identical $I_3 = I_4 = I_{\text{mid}}$, and solving Eqs. (3.32) and (3.33) for $e^{-(V_c - V_{d1})}$ yields

$$e^{-(V_c - V_{d1})} = \frac{e^{\kappa(V_c - V_1)}}{e^{\kappa(V_c - V_1)} + e^{\kappa(V_c - V_2)}} \tag{3.34}$$

Substituting the term from Eq. (3.34) into Eq. (3.33) and from Kirchhoff's current law (KCL)

$$I_b = I_1 + I_2 + I_{\text{mid}} \tag{3.35}$$

$$= I_0\, e^{\kappa(V_c - V_1)} + I_0\, e^{\kappa(V_c - V_2)} + S \cdot I_0\, e^{\kappa(V_c - V_2)} \frac{e^{\kappa(V_c - V_1)}}{e^{\kappa(V_c - V_1)} + e^{\kappa(V_c - V_2)}} \tag{3.36}$$

$$\Rightarrow e^{\kappa V_c} = \frac{I_b}{I_0 \cdot (e^{-\kappa V_1} + e^{-\kappa V_2}) + S \cdot I_0 \frac{e^{-\kappa V_1} \cdot e^{-\kappa V_2}}{e^{-\kappa V_1} + e^{-\kappa V_2}}} \tag{3.37}$$

The antibump outputs sum together to

$$I_{\text{sum}} = I_1 + I_2 = I_b - I_{\text{mid}} = I_0\, e^{\kappa(V_c - V_1)} + I_0\, e^{\kappa(V_c - V_2)} \tag{3.38}$$

$$= \frac{I_b}{I_0 + S \cdot I_0 \frac{e^{-\kappa V_1} \cdot e^{-\kappa V_2}}{\left(e^{-\kappa V_1} + e^{-\kappa V_2}\right)^2}} \tag{3.39}$$

Using $V_2 = V_1 - \Delta V$, the term in the denominator of Eq. (3.39) can be simplified

$$\frac{e^{-\kappa V_1} \cdot e^{-\kappa V_2}}{\left(e^{-\kappa V_1} + e^{-\kappa V_2}\right)^2} = \frac{e^{\kappa \Delta V}}{\left(1 + e^{\kappa \Delta V}\right)^2} \tag{3.40}$$

[1] Note that the terminal voltages are given in units of the thermal voltage U_T.

Dividing the nominator and denominator of Eq. (3.40) by $e^{\kappa\Delta V/2}$ yields

$$\frac{1}{\left(e^{\kappa\Delta V/2}+e^{-\kappa\Delta V/2}\right)^2} = \frac{4}{\cosh^2\left(\frac{\kappa\Delta V}{2}\right)} = 4\,\mathrm{sech}^2\left(\frac{\kappa\Delta V}{2}\right) \tag{3.41}$$

$$\text{with} \quad \cosh(x) = \frac{e^x - e^{-x}}{2},\ \mathrm{sech}(x) = \frac{1}{\cosh(x)} \tag{3.42}$$

Using this relation, Eq. (3.39) can be simplified and we get

$$I_{\text{sum}} = \frac{I_b}{1+\frac{S}{4}\,\mathrm{sech}^2\left(\frac{\kappa\Delta V}{2}\right)} \tag{3.43}$$

where the voltages are in U_T units. $U_T = kT/q = 25.4$ mV.

When $\Delta V = 0$, the cosh term is 1 and the antibump output sums to

$$I_{\text{sum,DC}} = I_1 + I_2 = \frac{I_b}{\frac{S}{4}+1} \tag{3.44}$$

This is the DC current component of the output signal of the squaring circuit and will be removed in the subsequent band-pass stage.

The antibump output current ranges from the minimum value in Eq. (3.44) for $\Delta V = 0$ to the maximum value I_b when the middle branch is shut off. Hence, the dynamic range (the ratio of the maximum to the minimum current) is $\frac{S}{4}+1$ (see Table 3.2). It is reported in [11] (p. 172) that for very large S, the bottom of the antibump output characteristic becomes very flat. This contrasts with the requirement of a characteristic of a parabolic curve and sets a ceiling on S.

Transient analysis in T-Spice has shown an AC signal amplitude at the preamplifier output in the order of 250 mV. This sets the range of input voltages where the I–V characteristic should have a parabolic form and should not be saturated. Moreover, the DC current of the antibump circuit $I_{\text{sum,DC}}$ was minimized without losing the quadratic shape. All these considerations led to the final strength ratio of $S = 64$. Fig. 3.7 shows the simulated sweep input-to-output characteristic of the antibump circuit. The theoretical form for I_{sum} fits the data quite well.

Since the antibump circuit has a differential input, the circuit behavior is approximately independent of the common-mode voltage or the DC level of the input voltage which is set by the reference voltage of the OpAmp of the preceding preamplifier stage. In reality, the non-zero conductance of the bias transistor in the current mirror causes a larger bias current with decreasing common-mode input voltage.

3.2.3 Practical Considerations

Because of short and narrow channel effects, doubling the length of a transistor is not equal to putting two transistors in series. Therefore it is crucial to use unit transistors in series and parallel in the antibump circuit to implement a certain

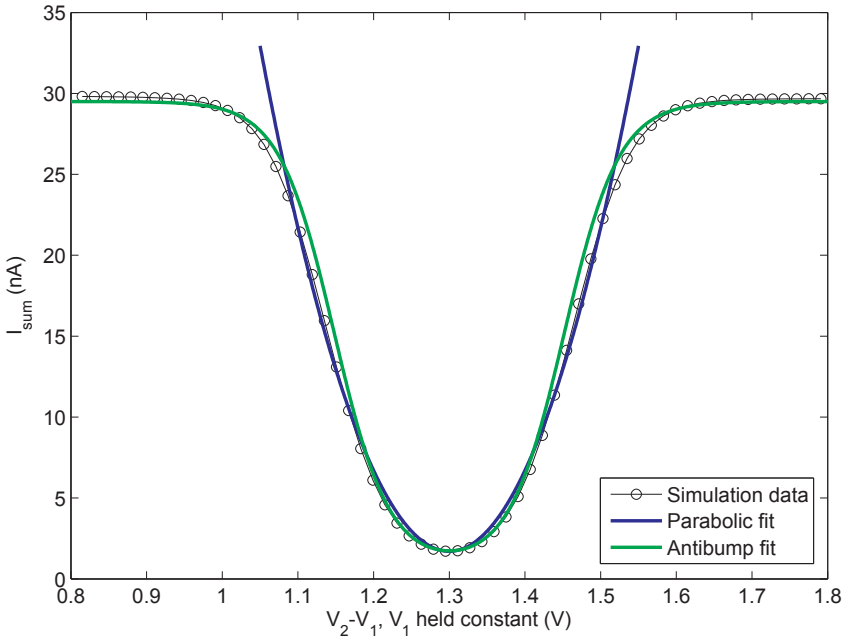


Figure 3.7: Input-to-output I–V characteristic of the antibump circuit. The plots show data point from simulation with T-Spice together with a theoretical fit with the antibump formula and a parabolic fit. V_1 was held constant and V_2 was swept over a range from 0.8 V to 1.8 V. The theoretical fit with the antibump formula in Eq. (3.43) was computed, using the parameters $I_b = 29.5$ nA, $S = 64$ and $\kappa = 0.7$. The parabolic fit is a result of computing the least-square fit of the simulation data. The theoretically fit curve of the antibump circuit and the simulation data are almost a perfect match. Since the numerically fit parabola matches the simulation data quite well, we conclude that the antibump circuit effectively approximates the squaring function.

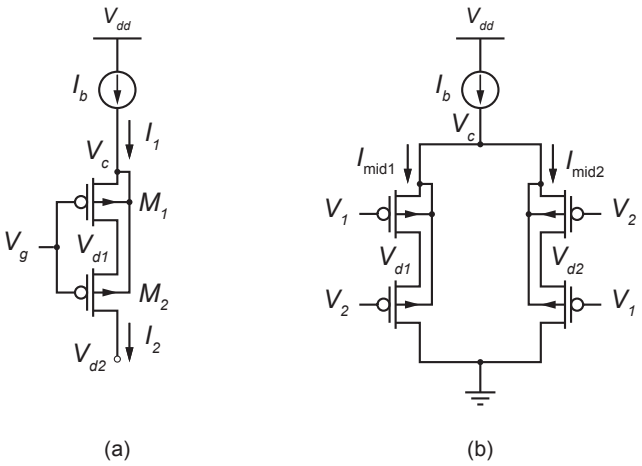


Figure 3.8: Schematics of the middle and outer legs of the antibump circuit. (a) Multiple transistors of the outer leg in series. (b) Multiple middle legs in parallel.

strength ratio (here $S = 64$). Consequently, all unit transistors are affected by these effects in the same way. The bulk is connected back to get rid of common-mode effects.

In the design of the antibump circuit, four transistors were put in series to increase to overall transistor length L. The following analysis aims at showing qualitatively that connecting two transistors in series is equivalent to doubling the length of a single transistor if the Early effect is neglected. Refer to Fig. 3.8 (a) for a sketch of the circuit topology under observation.

Obviously, the upper transistor, M_1, operates in the subthreshold triode region when the lower transistor, M_2, is stacked on M_1, and the equations for a transistor in the triode region apply. However, transistor M_2 is in the saturation region as usual and its drain potential can be neglected in the equation[2]

$$I_1 = I_0\, e^{\kappa(V_c - V_g)} \left(1 - e^{-(V_c - V_{d1})}\right), \quad I_2 = I_0\, e^{\kappa(V_c - V_g) - (V_c - V_{d1})} \tag{3.45}$$

Rearranging and substituting I_2 into the equation for I_1 in Eq. (3.45) gives

$$I_1 = I_0\, e^{\kappa(V_c - V_g)} - I_2 \tag{3.46}$$

Since the two transistors are stacked on each other, the drain currents must be identical $I_1 = I_2 = I$ and Kirchhoff's current law (KCL) holds. This yields

$$I = \frac{I_0}{2}\, e^{\kappa(V_c - V_g)} \tag{3.47}$$

[2]Note that the terminal voltages are given in units of the thermal voltage U_T.

Therefore, connecting two transistors in series is similar to doubling the length L of a single transistor.

The following analysis examines the effect of multiple middle legs in the antibump circuit with interchanged gate voltages. Again, the result is of purely qualitative nature because the Early effect is not taken into account. A major benefit of this circuit topology is the capability of balancing the Early effect and, especially, balancing it when the transistors are above threshold. The drain currents through the top and bottom transistors of the individual legs are given by[3]

$$I_{\text{mid1}} = S \cdot I_0\, e^{\kappa(V_c - V_1)} \left(1 - e^{-(V_c - V_{d1})}\right) = S \cdot I_0 \left(e^{\kappa(V_c - V_1)} - e^{\kappa(V_c - V_1) - (V_c - V_{d1})}\right) \tag{3.48}$$

$$I_{\text{mid1}} = S \cdot I_0\, e^{\kappa(V_c - V_2) - (V_c - V_{d1})} \tag{3.49}$$

$$I_{\text{mid2}} = S \cdot I_0\, e^{\kappa(V_c - V_2)} \left(1 - e^{-(V_c - V_{d2})}\right) = S \cdot I_0 \left(e^{\kappa(V_c - V_2)} - e^{\kappa(V_c - V_2) - (V_c - V_{d2})}\right) \tag{3.50}$$

$$I_{\text{mid2}} = S \cdot I_0\, e^{\kappa(V_c - V_1) - (V_c - V_{d2})} \tag{3.51}$$

The currents flowing through either leg must be equal according to KCL. Solving for $e^{-(V_c - V_{d1})}$ and $e^{-(V_c - V_{d2})}$ gives

$$e^{-(V_c - V_{d1})} = \frac{e^{\kappa(V_c - V_1)}}{e^{\kappa(V_c - V_1)} + e^{\kappa(V_c - V_2)}}, \quad e^{-(V_c - V_{d2})} = \frac{e^{\kappa(V_c - V_2)}}{e^{\kappa(V_c - V_1)} + e^{\kappa(V_c - V_2)}} \tag{3.52}$$

It is obvious by substituting the exponential terms in Eq. (3.52) into Eqs. (3.49) and (3.51) that I_{mid1} and I_{mid2} are identical

$$I_{\text{mid1}} = I_0 \cdot S \frac{e^{\kappa(V_c - V_2)} e^{\kappa(V_c - V_1)}}{e^{\kappa(V_c - V_1)} + e^{\kappa(V_c - V_2)}} \tag{3.53}$$

$$I_{\text{mid2}} = I_0 \cdot S \frac{e^{\kappa(V_c - V_1)} e^{\kappa(V_c - V_2)}}{e^{\kappa(V_c - V_1)} + e^{\kappa(V_c - V_2)}} \tag{3.54}$$

$$\Rightarrow I_{\text{mid1}} = I_{\text{mid2}} \tag{3.55}$$

Hence, doubling the number of middle legs is equal to doubling the width W of the transistors of a single leg.

3.2.4 Calculation of the Circuit Parameters

The strength ratio of the bump-antibump circuit is

$$S = \frac{2\,[\text{legs}] \cdot 8\,[\text{M}] \cdot (24/6)[\text{aspect ratio}]}{\frac{1}{4}\,[\text{stacked}] \cdot (24/6)\,[\text{aspect ratio}]} = 64 \tag{3.56}$$

where M is the number of identical fingers of a transistor. Neglecting parasitic effects, taking M fingers of the width W corresponds to an overall width of $M \cdot W$.

[3] Note that the terminal voltages are given in units of the thermal voltage U_T.

$I_b = 32.768$ nA
$S = 64$
$I_{\text{sum,DC}} = 1.71$ nA
Dynamic range = 25.6491 dB
$\kappa = 0.7$
$U_T = kT/q = 25.4$ mV

Table 3.2: Circuit parameters of the antibump circuit.

A least-square fit of the simulation data with a second order polynomial was computed as depicted in Fig. 3.7. The antibump output can be approximated by

$$I_{\text{sum}}(\Delta V) = 1.7048 \times 10^{-9} + 0.7069 \times 10^{-3} \cdot (\Delta V)^2 \text{ A} \tag{3.57}$$

In fact, in the intermediate region, where the difference of the input voltages $\Delta V = V_1 - V_2$ is small, the antibump circuit computes an approximation of the square of the differential input voltage ΔV, plus a DC offset $I_{\text{sum,DC}}$. The design parameters of the squaring circuit are summarized in Table 3.2.

3.3 Phoneme Band Filter

Current-mode circuits which can realize long time constants on the order of 1 s are required to filter the signal power in the phoneme band in the range of 2–16 Hz. The basic current-filtering topology examined here are first-order log-domain low-pass filters, as presented in [14], which are capable of fulfilling this requirement. The overall band-pass filtering function is achieved by consecutive low-pass and high-pass filters. As a matter of fact, the high-pass filter comprises of a circuit which forms the high-pass filtered signal by building the difference between the original input signal and the low-pass filtered signal by means of current mirrors.

The low-pass filter must be followed by the high-pass filter (and not vice versa). In contrast to the high-pass filter, the low-pass filtered signal current comes with a DC component which is needed to add another filter stage. A pure AC signal current, which results in the high-pass filter, could not be used for further processing. On the other hand, the input signal to the rectifier is ideally a pure AC signal which is either sourced or sunk by class-B current mirror.

3.3.1 Log-Domain Low-Pass Filter

The schematic of the selected first-order log-domain low-pass filter is shown in Fig. 3.9. In the following, the theoretical analysis of a p-type circuit, consisting only of pFETs, is shown, based on [14]. A p-type circuit topology has to be chosen to respect the fact that the input current from the preceding stage is sunk by

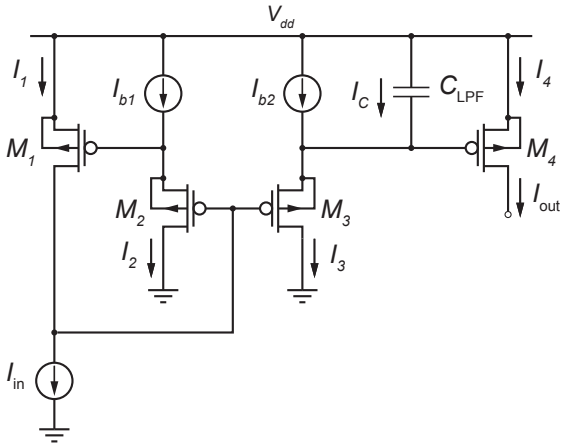


Figure 3.9: Schematic of the first-order log-domain low-pass filter.

a simple n-type current mirror and to protect the low-current nodes from later contamination from parasitic photocurrents [15] when this circuit is integrated with vision chips. As an advantage, the potentials of the n-wells can be set arbitrarily in the single-tub target process to the respective source potential of the pFETs, thus, eliminating the κ-effect (backgate effect or body effect).

The lowpass filtering function is implemented by transistors M_1–M_4 and capacitor C_{LPF}. Additionally, cascode transistors could be used to keep the drain voltages of M_1 and M_4 equal but were omitted in this design in order to reduce the complexity.

The basic assumption made is that the dynamics of the circuit are dominated by the presence of the pole caused by C_{LPF}. The poles originating from parasitic capacitance at the input and output nodes are supposed to be at much higher frequencies than the ones of interest. Assuming that all transistors, M_1–M_4, work in the subthreshold saturation region, the transistor equations are

$$I_1 = I_0\, e^{-\kappa V_{gs1}/U_T}, \quad I_2 = I_0\, e^{-\kappa V_{gs2}/U_T}, \tag{3.58}$$

$$I_3 = I_0\, e^{-\kappa V_{gs3}/U_T}, \quad I_4 = I_0\, e^{-\kappa V_{gs4}/U_T} \tag{3.59}$$

where κ is the subthreshold slope factor (for a pFET), I_0 is the transistor's off current (process dependent) and $U_T = kT/q = 25.4$ mV is the thermal voltage [11]. From Kirchhoff's voltage law (KVL) around the loop Gnd, M_1–M_4, Gnd

$$V_{gs1} + V_{gs2} = V_{gs3} + V_{gs4} \tag{3.60}$$

Multiplying the currents I_1, I_2 and I_3, I_4 gives the equations

$$I_1 \cdot I_2 = I_0\, e^{-\kappa (V_{gs1}+V_{gs2})/U_T} \tag{3.61}$$

$$I_3 \cdot I_4 = I_0\, e^{-\kappa (V_{gs3}+V_{gs4})/U_T} \tag{3.62}$$

respectively. From Eq. (3.60), it is apparent that the two products in Eqs. (3.61) and (3.62) are equal, and the translinear equation for this circuit can be derived

$$I_1 \cdot I_2 = I_3 \cdot I_4 \tag{3.63}$$

From Kirchhoff's current law (KCL) at either the source or drain terminals of the transistors M_1–M_4,

$$I_1 = I_{\text{in}} \tag{3.64}$$
$$I_2 = I_{b1} \tag{3.65}$$
$$I_3 = I_{b2} + I_C \tag{3.66}$$
$$I_4 = I_{\text{out}} \tag{3.67}$$

and we find that the translinear equation (3.63) can be rewritten including the newly found relations

$$I_{\text{out}} \cdot (I_{b2} + I_C) = I_{\text{in}} \cdot I_{\text{b1}} \tag{3.68}$$

The current through capacitor C_{LPF} is

$$I_C = C_{\text{LPF}} \cdot \dot{V}_C \qquad \text{with} \quad (\dot{\cdot}) = \frac{\text{d}}{\text{dt}} \tag{3.69}$$

Taking the first derivative with respect to time of I_4 in Eq. (3.59), and substituting I_4 into the equation gives

$$I_4 = I_0\, e^{\kappa V_C/U_T} \quad \Rightarrow \quad \dot{I}_4 = \frac{I_0\kappa}{U_T}\, e^{\kappa V_C/U_T} \cdot \dot{V}_C = \frac{I_4\kappa}{U_T} \cdot \dot{V}_C \tag{3.70}$$

Solving Eq. (3.70) for $\dot{V}_C$ and substituting it into Eq. (3.69) yields

$$\dot{V}_C = \frac{U_T}{\kappa} \cdot \frac{\dot{I}_4}{I_4} \tag{3.71}$$
$$\Rightarrow \quad I_C = C_{\text{LPF}} \cdot \frac{U_T}{\kappa} \cdot \frac{\dot{I}_4}{I_4} \tag{3.72}$$

As a consequence, substituting Eq. (3.72) into the translinear equation (3.68) and using $I_4 = I_{\text{out}}$ results in the following time domain differential equation

$$I_{\text{out}} \cdot I_{b2} + \dot{I}_{\text{out}} C_{\text{LPF}} \cdot \frac{U_T}{\kappa} = I_{\text{in}} \cdot I_{b1} \tag{3.73}$$

Thus, the transfer function of the circuit in the Laplace domain is

$$H_{\text{LPF}}(s) = \frac{I_{\text{out}}}{I_{\text{in}}} = \frac{I_{b1}}{I_{b2} + s\frac{C_{\text{LPF}}U_T}{\kappa}} = \frac{I_{b1}/I_{b2}}{1 + s\frac{C_{\text{LPF}}U_T}{\kappa I_{b2}}} \tag{3.74}$$
$$= \frac{A_{\text{I,dc}}}{1 + \frac{s}{\omega_0}} \qquad \text{with} \quad A_I = I_{b1}/I_{b2}, \quad \omega_0 = 2\pi f_0 = \frac{1}{\tau_0} = \frac{\kappa I_{b2}}{C_{\text{LPF}}U_T} \tag{3.75}$$

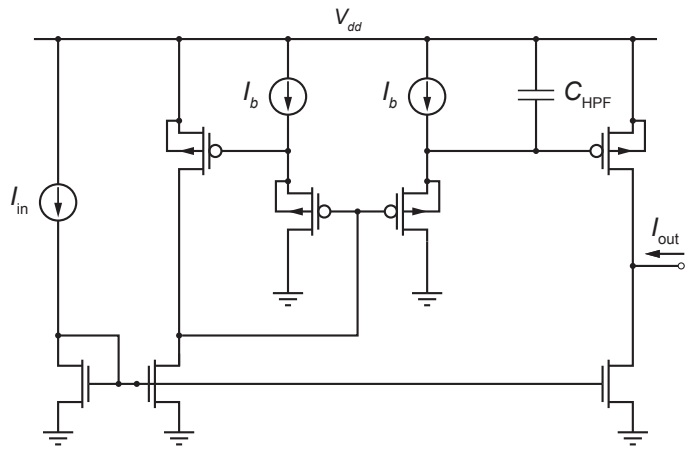


Figure 3.10: Schematic of the first-order log-domain high-pass filter.

which describes a first-order low-pass filter with DC current gain $A_{\mathrm{I,DC}}$ and 3-dB cutoff frequency $\omega_0 = 1/\tau_0$. It is evident that the DC current gain is given by the ratio of the bias currents I_{b1}/I_{b2} and that the time constant of the low-pass filter is governed by I_{b2} only.

Solving Eq. (3.75) for the bias current I_{b2}, which determines the pole, gives

$$I_{b2} = \frac{C_{\mathrm{LPF}} U_T}{\kappa \tau_0} = \frac{2\pi f_0 C_{\mathrm{LPF}} U_T}{\kappa} \tag{3.76}$$

Refer to Fig. 3.11 for a plot of the tranfer characteristic of the low-pass filter.

3.3.2 Log-Domain High-Pass Filter

The high-pass filter is implemented by taking the difference between the low-pass filtered input signal and the input signal itself (see Fig. 3.10). The filtered current is ideally subtracted from a mirrored replica of the input current. As a side benefit, the carrier DC signal is removed by the subtraction and solely the AC signal is left.

Consequently, the transfer function of the low-pass filter has to be subtracted from one

$$H_{\mathrm{HPF}}(s) = 1 - H_{\mathrm{LPF}}(s) \tag{3.77}$$

Setting $I_{b1} = I_{b2} = I_b$ in the transfer function of the low-pass filter $H_{\mathrm{LPF}}(s)$, Eq. (3.74) results in the following Laplace domain transfer function

$$H_{\mathrm{HPF}}(s) = \frac{1 - \left(1 + \frac{s}{\omega_0}\right)}{1 + \frac{s}{\omega_0}} = -\frac{\frac{s}{\omega_0}}{1 + \frac{s}{\omega_0}} \tag{3.78}$$

$$\text{with} \quad \omega_0 = 2\pi f_0 = \frac{1}{\tau_0} = \frac{\kappa I_b}{C_{\mathrm{HPF}} U_T} \tag{3.79}$$

The zero corner frequency in the transfer function of the high-pass filter corresponds to the pole in the transfer function of the low-pass filter. Again, the bias current I_b is

$$I_b = \frac{C_{\mathrm{HPF}} U_T}{\kappa \tau_0} = \frac{2\pi f_0 C_{\mathrm{HPF}} U_T}{\kappa} \tag{3.80}$$

Refer to Fig. 3.11 for a Bode plot of the transfer characteristic of the high-pass filter.

Since the difference between a copy of the original signal and the output signal is built, it is crucial to obtain a unity DC current gain in the high-pass filter. Therefore, the two bias currents I_{b1} and I_{b2} must be equal. Transistor mismatches and current inequalities might cause a deviation of the unity gain of the high-pass filter leading to DC offsets, which in turn can jeopardize the correct behavior of the filter. As a remedy, a leakage transistor is incorporated in the neuron to eliminate these offsets.

3.3.3 Log-Domain Band-Pass Filter

The first-order band-pass filter is built of a log-domain low-pass filter and a log-domain high-pass filter in series. Therefore, the overall band-pass filter frequency response is determined by the product of the two transfer functions of the individual filters

$$H_{\mathrm{BPF}}(s) = H_{\mathrm{LPF}}(s) \cdot H_{\mathrm{HPF}}(s) \tag{3.81}$$

The bode plot of the tranfer function of the band-pass filter is depicted in Fig. 3.11. The bias currents of the band-pass filter and in general are powers of two of 1 pF. Independent of the accuracy of the size of the master bias current, the ratio of the corner frequencies of the band-pass filter and thus the bandwidth is preserved assuming that all the bias currents are off by the same amount.

3.3.4 Calculation of the Circuit Parameters

A trade-off between the capacitor area and the smallest current that the bias generator can provide has to be made. The implication of Eqs. (3.75) and (3.79) is that the larger we make the filter capacitor, the greater the bias current can be in order to obtain the same cutoff frequency. Power constraints are not an issue this time as these tiny currents scarcely contribute to the total power consumption.

Substituting the design parameters into Eq. (3.75), for a 16 Hz cutoff frequency with $C_{\mathrm{LPF}} = 10$ pF, $\kappa = 0.7$, and $U_T = 25.4$ mV, the bias current I_{b2} should be

$$I_{b2} = \frac{2\pi f_c C_{\mathrm{LPF}} U_T}{\kappa} = 36.5 \text{ pA} \tag{3.82}$$

The gain in the pass-band of the high-pass filter can be controlled by the ratio of the two bias currents I_{b1}/I_{b2} in the low-pass stage. We opt for a gain of 2, thus the

$C_{\mathrm{LPF}} = 10$ pF
$f_c = 16$ Hz
$I_{b2} = 36.5$ pA
$I_{b1} = 73.0$ pA
$\kappa = 0.7$
$U_T = kT/q = 25.4$ mV

$C_{\mathrm{HPF}} = 10$ pF
$f_c = 2$ Hz
$I_b = 4.56$ pA
$\kappa = 0.7$
$U_T = kT/q = 25.4$ mV

Table 3.3: Circuit parameters of the band-pass filter.

current I_{b1} is given by

$$I_{b1} = 2 \cdot I_{b2} = 73.0 \text{ pA} \tag{3.83}$$

For a 2 Hz corner frequency with $C_{\mathrm{HPF}} = 10$ pF, $\kappa = 0.7$, and $U_T = 25.4$ mV, the bias current I_b should be

$$I_b = \frac{2\pi f_c C_{\mathrm{HPF}} U_T}{\kappa} = 4.56 \text{ pA} \tag{3.84}$$

Table 3.3 lists all design parameters required for the simulation and design of the first-order log-domain band-pass filter.

3.3.5 Simulation Results

Bode plots of all the transfer characteristics of the low-pass, high-pass and band-pass filters are depicted in Fig. 3.11. Taking the deviation of the bias currents from the ideal value caused by the finite resolution of the bias generator into account, good equivalence between the theoretically derived and simulated data is seen, at least in these simulations.

3.4 Half-Wave Current Rectifier

The phoneme power must be rectified prior to averaging of the signal in the silicon neuron. A well-suited circuit for that purpose is a class-B current mirror with active feedback as described in [16, 17], which provide a more elaborate analysis, especially about dead-zone reduction in the rectifier. A class-B mirror is a current structure which operates to mirror either positive or negative current from a single node and thus performs half-wave rectification only. The circuit is depicted in Fig. 3.12. The rectifier output current is the negative half wave which corresponds to $I_{\mathrm{out}} = -I_{\mathrm{in}}$ and has ideally zero DC offset. An OTA for active feedback is required to even rectify signals with a small amplitude and a short period. Otherwise the associated capactitance of the input node could not be charged fast enough and the input devices, either M_1 or M_2, would not turn on.

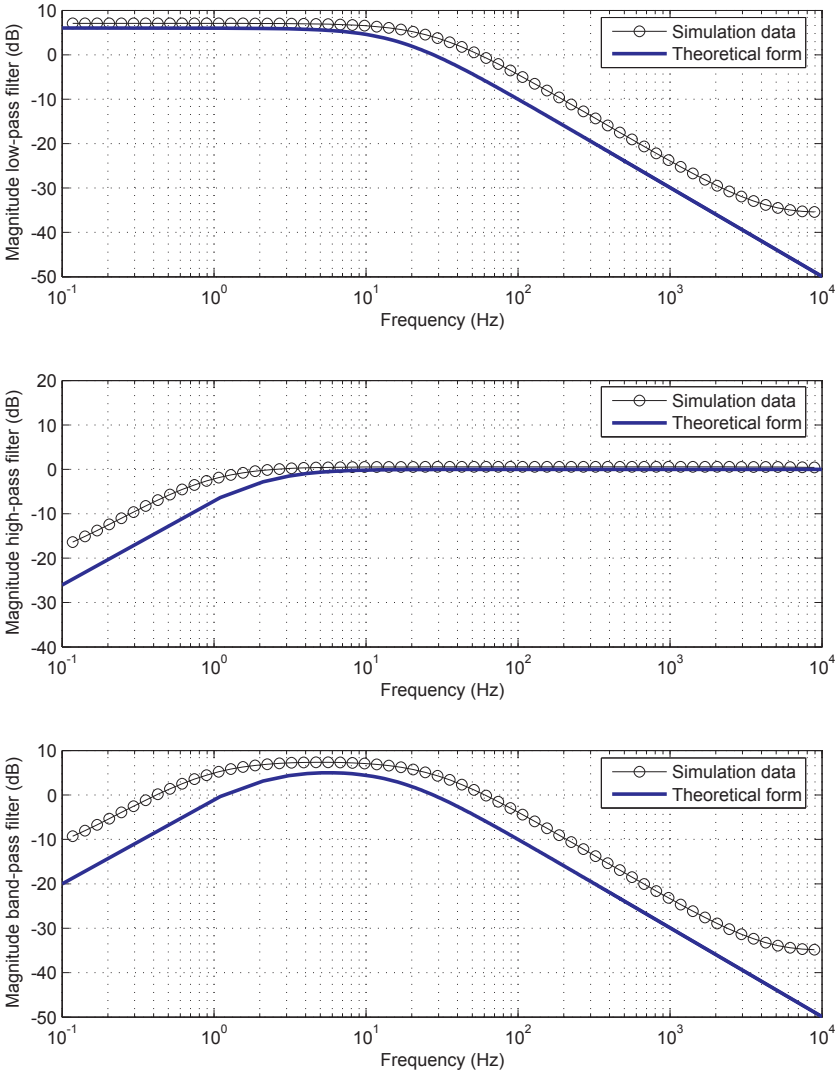


Figure 3.11: Bode plots (magnitude) of the low-pass, high-pass and band-pass filters (from top to the bottom). It is confirmed that the calculated bias currents effectively lead to the required band-pass characteristic. Deviations from the theoretical form can be explained by the discrepancy between the bias current used in the derivation and the bias currents provided by the bias generator.

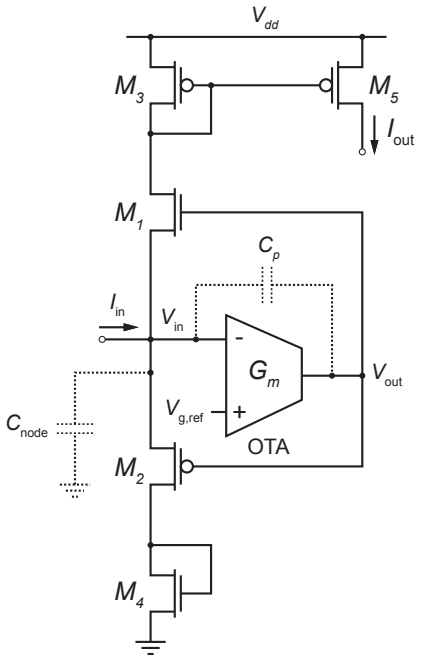


Figure 3.12: Schematic of the class-B current mirror with active feedback.

3.4.1 Qualitative Analysis of the Class-B Current Mirror

A class-B current mirror is capable of sourcing and sinking current from the input I_{in} and mirroring it to the output I_{out}. The current I_{in} is considered to be positive, if it flows into the circuit. The input transistors, M_1 and M_2 in Fig. 3.12, are both shut off, if no current is applied to the input node. Large input voltages are required to turn the input transistors, behaving like subthreshold diode-like devices, on. Hence, a voltage dead zone or turn-on region is present at the input, such that little current is output by I_{out} until I_{in} has changed significantly. The voltage dead zone consists of the sum of the nFET and pFET diode drops of the input transistors and is process-dependent. In [16] it is reported to be 2.2 V_{pp} peak-to-peak.

This dead zone might be a problem for low-current systems which cannot charge any parasitic node capacitance quickly enough. As a result, the input transistors fail to turn on, causing the rectification to fail. Active feedback attempts to reduce the turn-on voltages at the input node as shown in Fig. 3.12. The feedback amplifier with gain A attempts to clamp V_{in} at $V_{\text{g,ref}}$ by controlling the gate voltages of M_1 and M_2. Since the amplifier needs to drive only capacitive loads, i.e. the gates of the transistors M_1 and M_2, an OTA was chosen. [16] shows that the minimum detectable current amplitude $I_{\text{in,min}}$ is given by

$$I_{\text{in,min}} = \omega \cdot \left(C_p + \frac{C_{\text{node}}}{A} \right) \cdot \frac{V_D}{2} \approx \omega \cdot C_p \cdot \frac{V_D}{2} \tag{3.85}$$

$I_b = 100$ pA
$V_{\text{g,ref}} = 1.65$ V

Table 3.4: Circuit parameters of the class-B current mirror.

where ω is the input frequency, C_p is the gate-to-source parasitic capacitance of M_1 and M_2, C_{node} is due to the output filter capacitance and node parasitics, A is the voltage gain of the feedback amplifier, and the dead-zone voltage V_D is a constant peak to peak. Reportedly, the effect of dead-zone reduction is limited by parasitics if the gain of the amplifier is increased.

3.4.2 Circuit Parameters

The OTA for the active feedback in Fig. 3.12 was biased with 100 pA. The reference voltage of the OTA was set half-rail at 1.65 V. The design parameters of the class-B current mirror are listed in Table 3.4.

3.5 Low-Power I&F Neuron

The leaky low-power neuron from [18] was redesigned and implemented because it converts the current signal into a voltage and is in agreement with the main requirement of low power. A schematic of the Integrate-and-Fire (I&F) neuron is shown in Fig. 3.13. The injection current to the neuron represents the signal power in the phoneme modulation band. It is averaged over time and integrated on the membrane capacitor C_{mem}. At the same time, undesirable high-frequency signals and noise are cancelled. When the membrane potential reaches a certain level, a spike is generated at the output. The output spiking signal V_s is a digital signal which acts as a wake-up signal for the following microcontroller.

An additional leakage transistor, M_{17}, was added which attempts to compensate the DC mismatch caused by the preceding phoneme band-pass filter and the rectifier. Therefore, input currents that do not exceed the leakage current do not affect the membrane potential. In order to avoid coupling from the spiking neuron back to the rectifier through the Miller effect, a cascode transistor, M_{16}, was added to the input current mirror. All n-wells are tied to V_{dd}. The adaptation mechanism was omitted.

3.5.1 Working Principle

[19] describes that the injection current I_{inj} is linearly integrated by C_{mem} onto V_{mem}. Because transistors M_1–M_2 form a source-follower, V_{in} increases along with V_{mem}. As soon as V_{in} reaches the threshold of the first inverter, the first inverter starts to switch and a positive feedback current I_{fb} charges the membrane capacitor

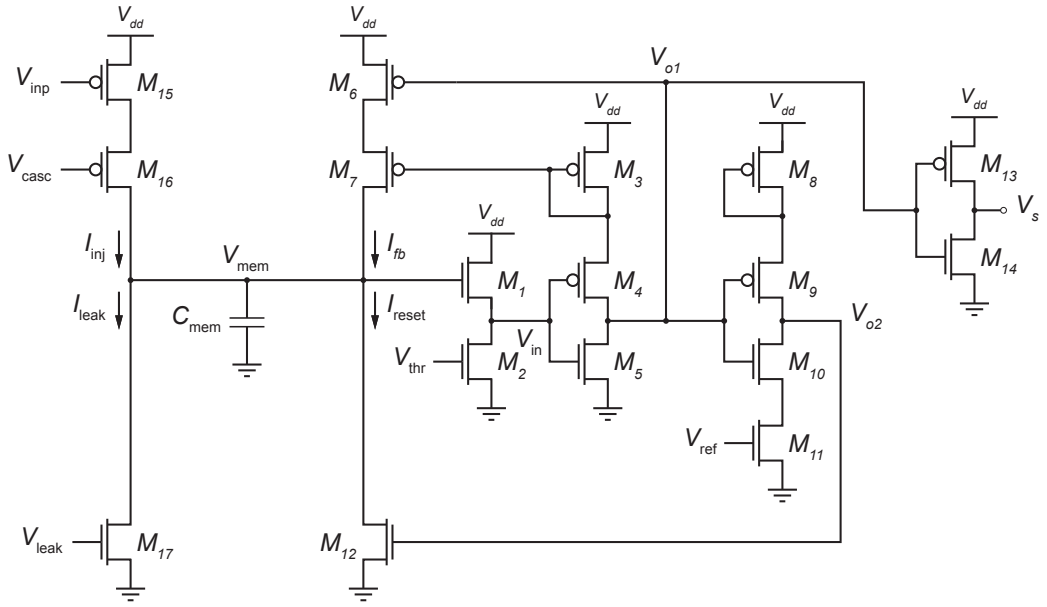


Figure 3.13: Schematic of the low-power I&F neuron.

$V_{\text{thr}} = 0.529$ V
$V_{\text{ref}} = 0.47$ V
$C_{\text{mem}} = 1$ pF

Table 3.5: Circuit parameters of the I&F neuron.

C_{mem} even more rapidly, thus reducing the switching time and the power consumption of the inverter.

When V_{mem} is large enough to make the first inverter switch, a spike is generated and V_s and V_{o2} are driven to V_{dd}. At the same time, the reset transistor, M_{12}, is fully turned on, and C_{mem} is quickly discharged, forcing V_{mem} to go to ground. V_{o1} goes back to V_{dd} and M_{10} is turned on. A current controlled by V_{ref} then discharges node V_{o2} through the path M_{10}–M_{11}. In fact, this inverter is a starved inverter because the maximum switching current is determined by the bias voltage of M_{11}. As long as V_{o2} is sufficiently high to turn on M_{12}, the membrane potential V_{mem} is tied to ground. This time is called the "refractory" period and the neuron cannot spike. The design parameters of the I&F neuron are listed in Table 3.5.

Since the change in the current per time dI/dt is quite large when the neuron spikes, the affected transistors are connected to DigVdd and DigGnd and led to separate pads.

Name	Ideal current	$(W/L)_{\text{biasgen}}$ [λ]	Eff. current	$(W/L)_{\text{sd}}$ [λ], M
Ib1OpAmpPreamp	2.048 nA	12/16	1.85 nA	20/16, 10
Ib2OpAmpPreamp	524.288 nA	12/16	548 nA	20/16, 10
IbOTAPreamp	8 pA	6/24	7.62 pA	
IbOTASquaring	1 pA	6/24	1.05 pA	
IbSquaring	32.768 nA	24/24	29.5 nA	
Ib1Lowpass	128 pA	24/6	119 pA	
Ib2Lowpass	64 pA	24/6	59.5 pA	
IbHighpass	2 pA	24/6	1.98 pA	
IbOTARectifier	128 pA	6/24	119 pA	
VCascNeuron	8.192 nA	10/10	7.29 nA	
VLeakNeuron	1 pA	24/6	1.11 pA	
VThrNeuron	8.192 nA	10/10	7.3 nA	
VRefNeuron	2.048 nA	10/10	1.85 nA	

Table 3.6: Bias generator currents. The ideal and effective currents measured in the diode-connected mirror transistor in the bias generator during simulation are listed. Circuit parameter: $R_X = 120$ kΩ.

3.6 Bias Generator

A fixed bias generator from [20] is used on the chip. The entire speech detection circuit was simulated including the biasgen.

3.6.1 Bias Currents

The bias currents were made powers of two of 1 pA to avoid excessive resizing of the diode-connected transistor of the current mirror in the bias generator cell. The two bias currents of the OpAmp were multiplied by means of mirror multiplication by factors of 16. This cut-down of the current was necessary because the transistors in the bias generator providing the master current did not work in the saturation region with the targeted 3.3 V supply. Therefore, the master current had to be lowered. This allows a lower master current and thus a lower power consumption. 20 splitters and 1 termination cell were used. 13 bias currents were generated (max./min. bias currents 524.288 nA/1 pA (19 octaves, 5.7 decades)). The master current is 1.04858 μA. The resistor R_X was modified to approximately match the effective currents with those required and entered in the bias compiler. The currents set in the biasgen compiler and the effective currents measured during simulation are listed in Table 3.6. A small discrepancy between the corresponding currents is apparent.

Power consumption	Min.	Average	Max.	Unit
Speech detector	196.5	199.1	201.5	μW
Silicon neuron Vdd	–	2.9×10^{-3}	259.5	μW
Silicon neuron DigVdd	2.528×10^{-9}	3.116×10^{-3}	49.75	μW
Microphone preamplifier	196.4	198.9	201.3	μW
Bias generator	15.83	15.83	15.83	μW
Total	–	214.9	–	μW

Table 3.7: Power consumption of the speech detector measured after stable operating point is reached and during microphone input is active from 2.5 to 10 s.

3.7 Chip-Level Simulation Results Including Self-Biased Operation

A previously recorded sample for MATLAB was used for simulation. It is 7 seconds long and contains the phrase: "In pair with like car sounds [deep male voice]... (long silence) you're getting a lot of that [female voice]." The background sound consists of car sounds and noise. At around 6.5 seconds, the microphone was touched which caused an excitation with a step input (and power in the phoneme band) and the signal was wrongly classified as speech.

A transient analysis of the overall circuit including the bias generator was carried out and the results show a very good performance of the speech detector in terms of classification of speech/non-speech. Fig. 3.14 shows the processing of the full audio sample. Note that the start-up behavior is omitted in the plots. The spike trains are very well visible. The higher the spiking frequency, the more power the phoneme band contains. A plot with higher resolution is presented in Fig. 3.15. The simulation was done in two steps: First, the speech detector was simulated without the neuron, afterwards the neuron was simulated separately. The reason is that it takes a long simulation time to simulate the full circuit because the spiking neuron needs a high simulation resolution which reduces the simulation speed.

Table 3.7 shows the power consumption of the individual blocks. The total power consumption is 214.9 μW whereof 93 % are consumed in the speech detector. The microphone preamplifier burns 99 % of this power.

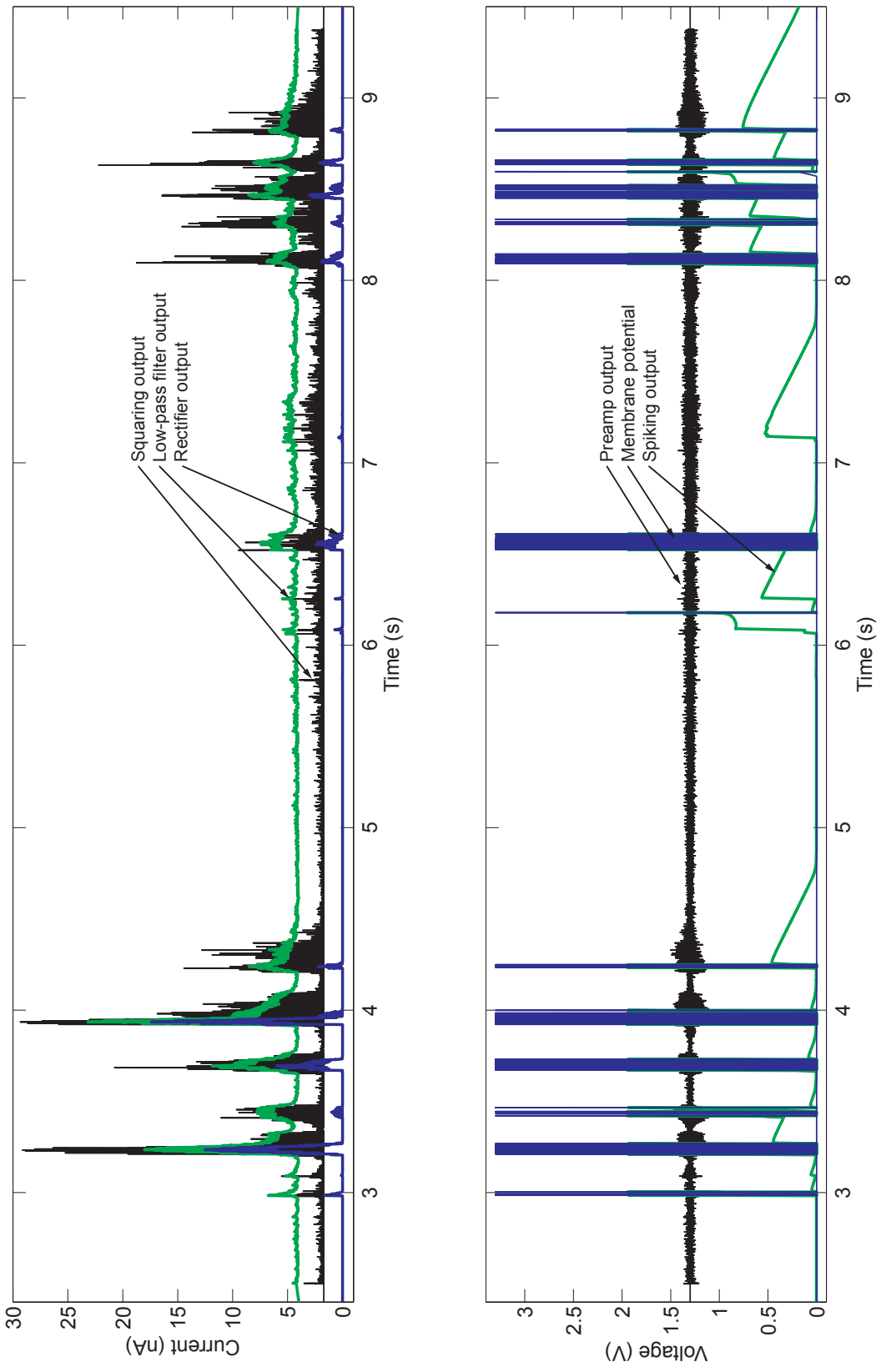


Figure 3.14: Chip-level simulation results of the speech detector.

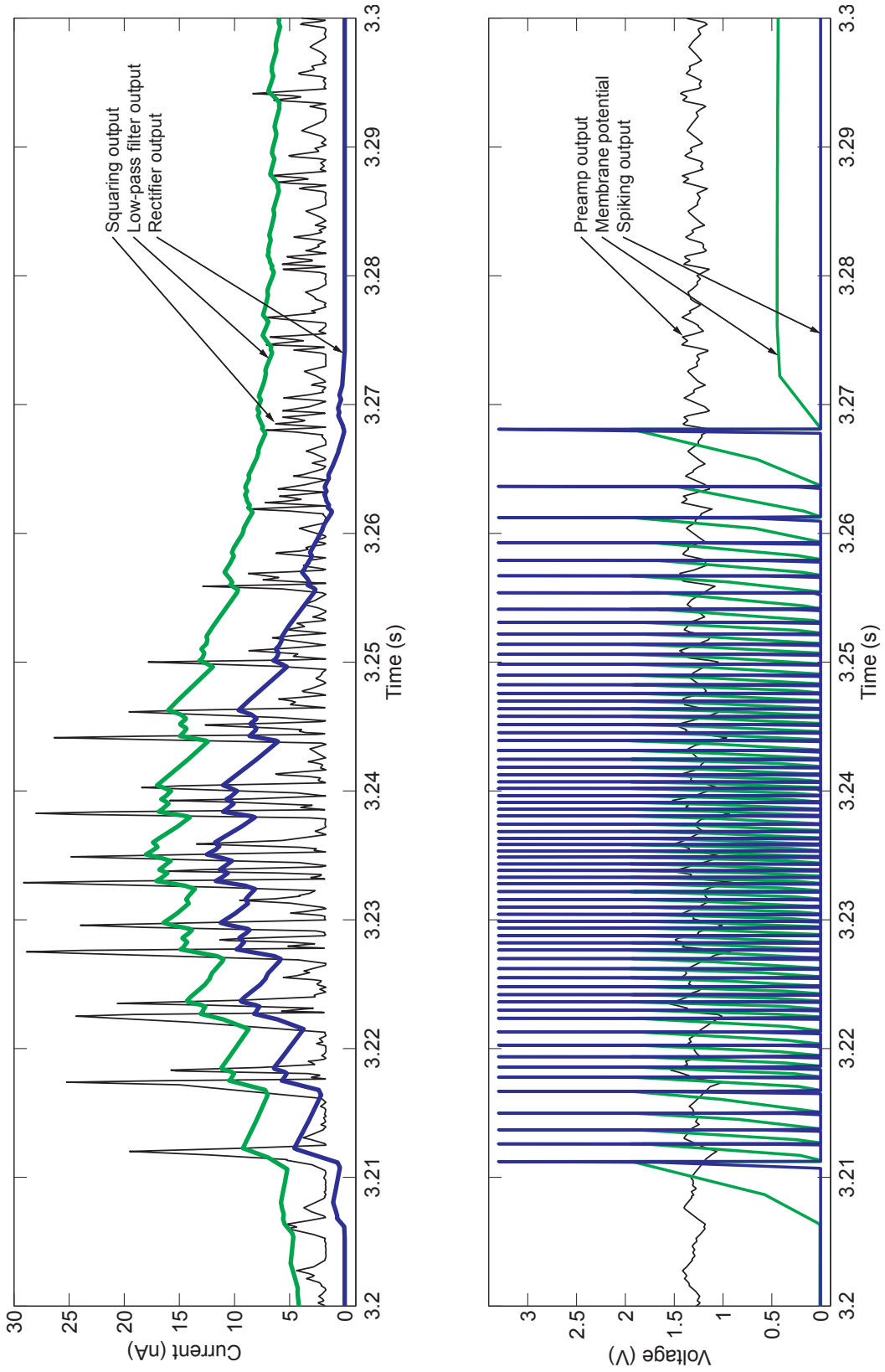


Figure 3.15: Chip-level simulation results of the speech detector (high resolution).

Chapter 4

Layout of the Speech Detector

In this chapter we give an overview of the layout of the speech detector. Layout techniques as well as EDA related issues are treated. A pin map is included to ease physical characterization of the prototype silicon.

4.1 General Issues

The chip was laid out and will be fabricated in the MOSIS 1.6 μm process (SCGA technology) which aims at a 5 V power supply. However, the speech detector circuitry was designed to work at 3.3 V only (Table 4.1).

A summary of project-specific guidelines which had to be respected is as follows:

- A metal2 shield is used which is the ground layer at the same time. We decided to use a metal shield because photodiodes will be incorporated into the circuit later on when the face and speech detection circuits will be combined. It is not necessary for the sake of the speech detector to work properly.

- The power supply line V_{dd} was given the highest priority, i.e. all other wires had to circumvent the V_{dd} wire by poly jumpers that were made 5 poly contacts (pcons) wide at maximum. Metal2 could not be used for that purpose as it forms the metal2 Gnd shield. V_{dd} carries high currents which would cause a voltage drop in the resistive poly layer. Correct circuit functionality could not be guaranteed. It does not matter for the bias voltages of the gate because

Parameter	
Process	MOSIS 1.6 μm (SCGA technology)
Power supply	typ. 3.3 V, max. 5 V
Layers	2 metal, 2 poly

Table 4.1: Process characteristics.

there are no currents once the gate has been charged. However, coupling of noise through the high-impedance node can alter the gate voltages.

- DigVdd and DigGnd lines were given the second priority.
- Gnd contacts were connected to the metal2 shield directly by means of vias, so hardly any Gnd wires can be found in the layout.
- Guard rings: 30λ ($\lambda = 0.8\ \mu$m) wide n-well guard rings surrounds the speech detector as well as the bias generator and are connected to V_{dd}. They absorb photo-generated minority carriers.
- A fixed cell height was chosen (where possible) to ease connections to the V_{dd} power supply bus.
- A wide V_{dd} bus is placed above the speech detector to contact the V_{dd} of all cells.

The layout methodology is important to ensure good device matching and circuit operation. This way, undesirable parasitic effects and coupling effects are minimized. Consequently, the physical characteristics will accord more closely with prediction from simulations. This is fundamental for the design of the speech detector where several arithmetic computations are successively carried out.

General considerations (partially taken from [11] (pp. 346–352) and [21]):

- Devices are placed in the same orientation to be subjected to the same processing variations. For example, the current propagation should be in the same direction.
- Common-centroid structures were used where practical (OpAmp, antibump circuit). A common symmetry center for matched devices was arranged to uniformly distribute the influences of gradients. However, the total area required is mainly increased due to additional routing.
- Dummy segments are placed on the ends of transistor arrays. The surrounding circuitry should be similar. Dummy transistors were connected in such a way that they do not draw current.
- Metal1 is not routed across the active gate area unless there is no other workaround because there have been reports that metal crossing channels increases mismatch.
- If the active area of a current mirror (e.g. in an OTA) needs to be crossed it should be done in an equal and symmetrical way, thus avoiding differential coupling effects.
- Multiple contacts are used to connect two different layers in order to reduce interlayer resistance (contact resistance $R_{\text{via}} = 0.06\ \Omega$, $R_{\text{poly}} = 27.5\ \Omega$).

- To avoid problems such as latch-up and substrate coupling, the potential of the substrate and wells has to be properly set by contact rings.
- The capacitors were made of a bottom poly1 plate and a top poly2 plate with the interpoly oxide as the insulator (sheet resistance $R_{\square} = 573$ aF/μm^2). Quadratic unit capacitor cells were used for a good matching of the filter time constants.
- Devices to be matched (e.g. transistors in differential pair, current mirror transistors) are placed close to one another because of the spatial variations of the process parameters.
- The power supplies of analog and digital circuits are separated. The switching of a digital signal can couple into an analog circuit and affect its operation.

4.2 Microphone Preamplifier

A common-centroid and compact solution was used for the layout of the differential pair of the OpAmp because matching is important not to cause systematic offsets. For the same reason, shorted dummy transistors were placed around the current mirrors in both types of OTAs in order to establish equal surroundings. To ensure good matching, the transistors of the differential pair and the current mirror are placed as close to one another as the design rules allow.

4.3 Squaring Circuit

Again, a common-centroid geometry was used for the layout of the antibump circuit (see Figs. 4.1 and 4.2). Since matched devices should have the same surroundings, dummy transistors were put on the edges of the common-centroid structure.

4.4 Silicon Neuron

The branches which carry high switching currents are connected to digital ground (DigGnd) and digital Vdd (DigVdd), respectively. The n-wells of the relevant pFETs are tied to DigVdd, too. Gnd and DigGnd as well as Vdd and DigVdd are separate voltage nets in the layout. However, PadGnd and Gnd are shorted whereas PadVdd is led to a pad and remains unconnected.

4.5 Padframe

The pad assignment was done according to the arrangement of the DollBrain (face detector) board to reuse the same PCB. However, since 16 pads (14 pads available) are needed to control the bias or reference voltages with the bias DAC, two outputs

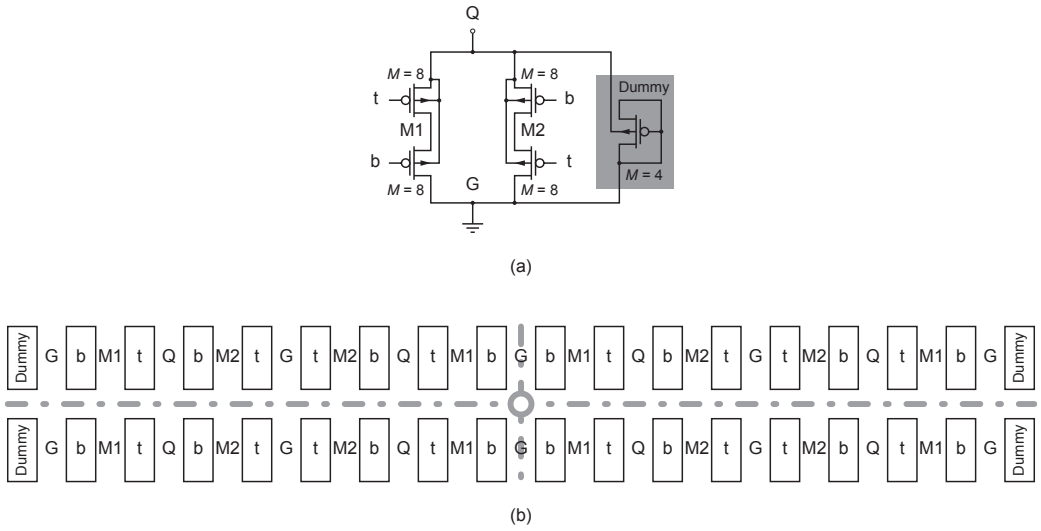


Figure 4.1: (a) Schematic of the middle leg of the antibump circuit. M denotes the number of parallel transistors. (b) Schematic view of the common-centroid structure as used in the antibump circuit. The dotted lines indicate the axes of symmetry. The boxes represent gate fingers.

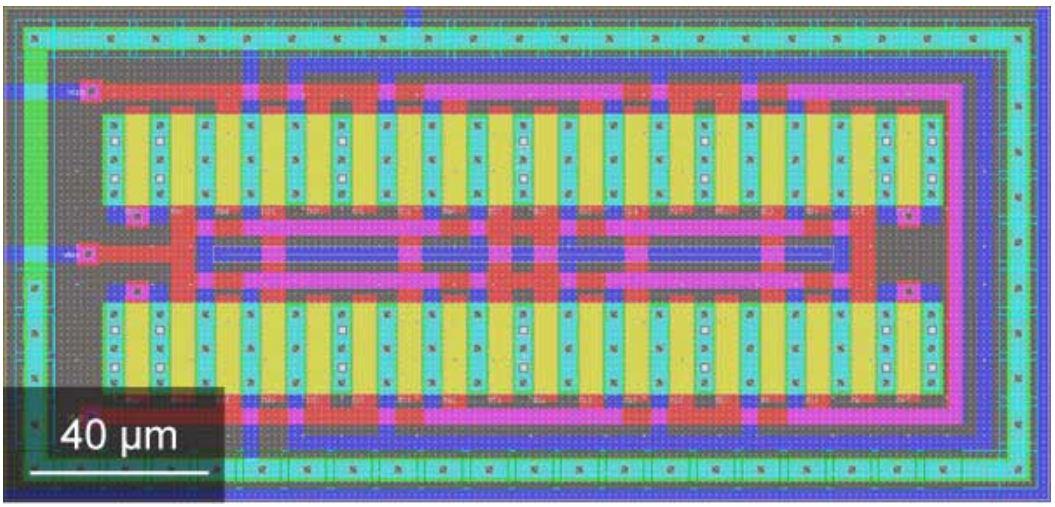


Figure 4.2: Layout of the antibump circuit. The common-centroid arrangement of the transistors of the middle leg is shown.

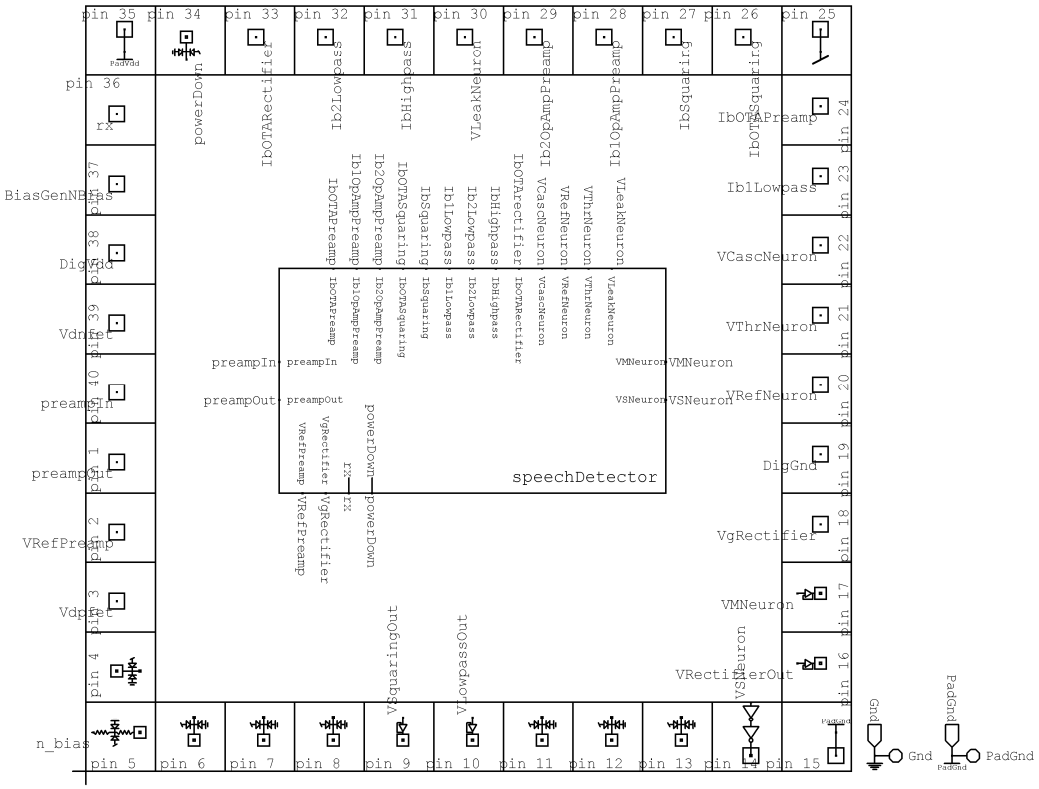


Figure 4.3: Padframe of the speech detector.

(pin no. 18 and 24) to the micro controller are used. 10 pads which lead to the pin header are required (9 pads available). Once again, a microcontroller output is used (pin no. 3). Fig. 4.3 shows an overview of the padframe.

The pad `n_bias` (follbias) supplies the bias voltages for the widepad unity-gain voltage buffers and is usually about 0.7 V. This bias voltage is not generated by the on-chip bias generator because it is only meant for debugging. It is not needed for a functionally correct working chip. If a pad is unused an input pad (inorpad) with electro-static discharge (ESD) protection is used.

4.5.1 Pin Description

All bias voltages are connected to the DAC which is capable of generating the required gate voltages in case the bias generator has to be overridden. Table 4.2 gives an overview of the pin map. The pin number, the signal name, the type of pad, the function and the board connection are listed along with the external wiring with discrete elements such as resistors. We decided to use an off-chip feedback resistor R_f in order to have more tolerance for debugging.

Pin no.	Name	Pad type	Board connection	Ext. connection
1	`preampIn`	barepad	PH JP4/2	Mic and R_s to Gnd
2	`VRefPreamp`	barepad	DAC	
3	`Vdpfet`	barepad	PH (former μC)	
4	`unused`	inorpad	μC	
5	`n_bias`	barepad	DAC	
6	`unused`	inorpad	μCLS	
7	`unused`	inorpad	μC	
8	`unused`	inorpad	μC	
9	`VSquaringOut`	widepad	PH JP4/4	
10	`VLowpassOut`	widepad	PH JP4/5	
11	`unused`	inorpad	μC	
12	`unused`	inorpad	μC	
13	`unused`	inorpad	μC	
14	`VSNeuron`	outpad	μC, PH JP4/6	
15	`PadGnd`	barepad		
16	`VRectifierOut`	widepad	PH JP4/7	
17	`VMNeuron`	widepad	PH JP4/8	
18	`VgRectifier`	barepad	DAC (former μC)	
19	`DigGnd`	barepad	PH JP4/9	
20	`VRefNeuron`	barepad	DAC	
21	`VThrNeuron`	barepad	DAC	
22	`VCascNeuron`	barepad	DAC	
23	`Ib1Lowpass`	barepad	DAC	
24	`IbOTAPreamp`	barepad	DAC (former μC)	
25	`Vdd`	barepad		
26	`IbOTASquaring`	barepad	DAC	
27	`IbSquaring`	barepad	DAC	
28	`Ib1OpAmpPreamp`	barepad	DAC	
29	`Ib2OpAmpPreamp`	barepad	DAC	
30	`VLeakNeuron`	barepad	DAC	
31	`IbHighpass`	barepad	DAC	
32	`Ib2Lowpass`	barepad	DAC	
33	`IbOTARectifier`	barepad	DAC	
34	`powerDown`	inorpad	μCLS	to Gnd
35	`PadVdd`	barepad		
36	`rx`	barepad		$R_X = 120$ kΩ
37	`BiasGenNBias`	barepad		10 pF to Gnd
38	`DigVdd`	barepad		
39	`Vdnfet`	barepad	PH JP4/3	
40	`preampOut`	barepad	PH JP4/1	$R_f = 300$ kΩ to pin 1

Table 4.2: Pin assignment of the speech detector chip. Notation: μC = microcontroller, μCLS = microcontroller (level shifter), PH = pin header.

Area	λ unit	mm^2 unit
Speech detector	$1725\lambda \times 480\lambda$	0.828 mm^2
Bias generator	$1913\lambda \times 587\lambda$	1.123 mm^2
Total		1.951 mm^2

Table 4.3: Area consumption of the speech detector ($\lambda = 0.8$ μm). The area required for routing between the speech detector and the bias generator and to the pads is not considered.

4.6 Bias Generator

The layout cell of the bias generator was automatically generated by a compiler [20] but for a slightly different technology. It was deliberately designed for a process with n- and p-select masks to make the layout portable. Before linking it to the speech detector, the parameter lambda per internal unit had to be rescaled from 1:200 to 1:1000. When the bias generator is linked to the speech detector, the layers must be mapped accordingly. However, the p-select layer was inherited but is not extracted for fabrication. Since the compiled bias generator was too wide, caused by the difference of bias current of several magnitudes, the master bias block and the rest of the bias generator circuit had to be split and were stacked on top of each other (see Fig. 4.4).

Moreover, a test structure consisting of a nFET and a pFET ($W/L = 24\lambda/6\lambda$) was included in the bias generator cell. The structure was placed in the vicinity of the master bias to take process variations into account and were covered by metal2 to make it insensitive to illumination. The common gate voltage and drain voltages of the transistors were brought off-chip to measure the individual bias currents during debugging. This circuitry allows to probe every bias current provided by the bias generator by connecting the bias voltage pad to the gate of the test transistors.

4.7 Design Rules

Active contacts must be surrounded by 1λ of select. To be on the safe side 2λ were chosen. This rule was not observed by the design-rule checker (DRC).

4.8 Layout Versus Schematic (LVS)

The layout speech detector was verified by a bottom-up approach. The layout of the chip is shown in Fig. 4.4. Table 4.3 gives an overview of the required chip area. It is almost ready for tape-out.

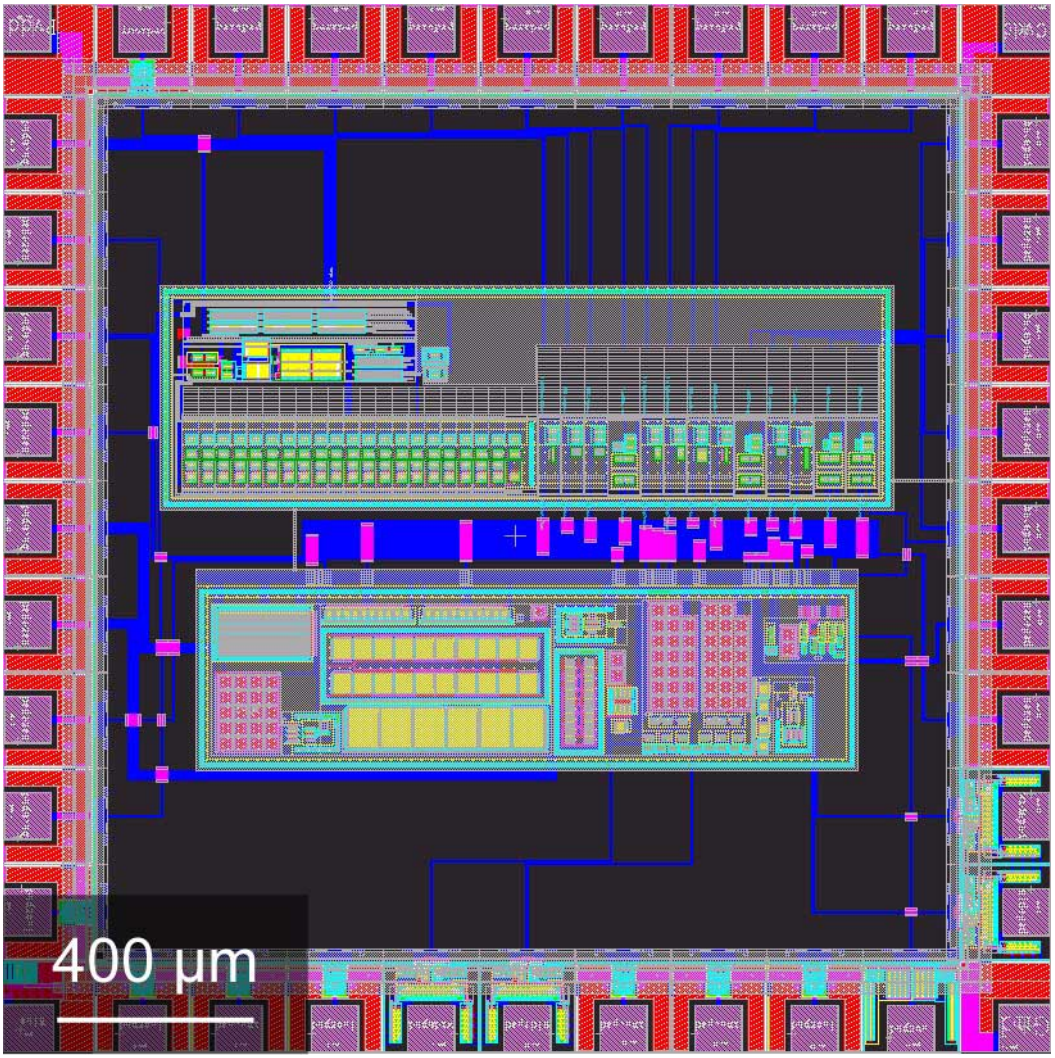


Figure 4.4: Chip layout.

Appendix A

Analysis of the Transfer Function of the Microphone Preamplifier

In this chapter we derive the transfer function of the microphone preamplifier in great detail. We discuss qualitatively the relevant poles, which are obtained in the analysis and determine the pass-band of the circuit, and indentify the circuit elements causing the poles.

A.1 Derivation of the Transfer Function

Until now, we have assumed that parasitic capacitances and output resistances are negligible (refer to Subsection 3.1.4 in Chapter 3). In practice, however, the parasitic capacitances have a significant effect on bandwidth. To recalculate the transfer function, the capacitances $C_{gs1}, C_{gd1}, C_{gd2}$ and the output resistances r_{o1}, r_{o2} are added to the circuit as shown in Fig. A.1.

To find a relationship between the equivalent microphone input voltage v_i and the output voltage of the microphone preamplifier v_o, Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL) can be applied at the nodes v_1, v_2, v_3 and around the OpAmp loop, respectively

$$(v_i - v_1)sC_{\text{mic}} + (v_2 - v_1)sC_{gd1} - v_1\left(\frac{1}{r_{\text{in}}} + sC_{gs1}\right) = 0 \tag{A.1}$$

$$(v_1 - v_2)sC_{gd1} - g_{m1}v_1 - g_{m2}v_3 + (v_3 - v_2)sC_{gd2} + \frac{v_o - v_2}{R_f} - \frac{v_2}{r_o} = 0 \tag{A.2}$$

$$-v_3 sC_{\text{ad,tot}} - \frac{v_3}{R_o} + G_m(v_2 - v_o) + (v_2 - v_3)sC_{gd2} = 0 \tag{A.3}$$

$$v_o + A(s) \cdot v_2 = 0 \tag{A.4}$$

where $r_o = r_{o1} \parallel r_{o2}$ is the output resistance of the JFET and the pFET of the adaptive element in parallel. This is a set of linear equations with four indepen-

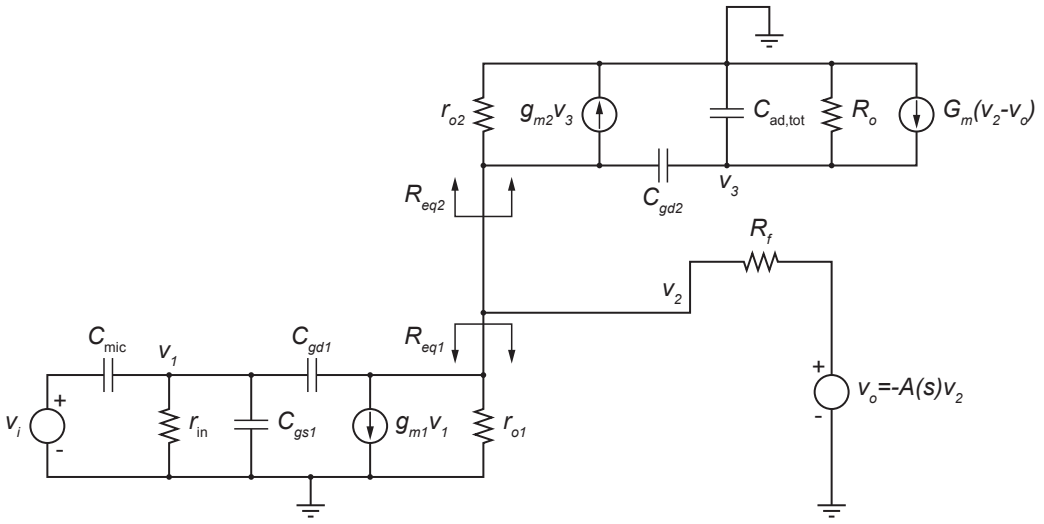


Figure A.1: Small-signal equivalent circuit for the microphone preamplifier.

dent variables. Note that the effective capacitance of the adaptive element $C_{\text{ad,tot}}$ comprises of the capacitance of the adaptive element C_{ad} itself, the gate-to-source capacitance C_{gs2} and the gate-to-bulk capacitance C_{gb2} of the pFET of the adaptive element

$$C_{\text{ad,tot}} = C_{ad} + C_{gs2} + C_{gb2} \tag{A.5}$$

Solving Eq. (A.4) for v_2 gives

$$v_2 = -\frac{v_o}{A(s)} \tag{A.6}$$

Substituting Eq. (A.6) into Eq. (A.1) and solving for v_1 yields

$$v_1 \left(s(C_{\text{mic}} + C_{gd1} + C_{gs1}) + \frac{1}{r_{\text{in}}} \right) = v_i \cdot sC_{\text{mic}} - \frac{v_o}{A} sC_{gd1} \tag{A.7}$$

$$\Rightarrow v_1 = \frac{v_i \cdot sC_{\text{mic}} - \frac{v_o}{A} sC_{gd1}}{s(C_{\text{mic}} + C_{gd1} + C_{gs1}) + \frac{1}{r_{\text{in}}}} \tag{A.8}$$

Solving for Eq. (A.3) for v_3 gives

$$v_3 \left(sC_{\text{ad,tot}} + \frac{1}{R_o} + sC_{gd2} \right) = -G_m v_o \left(1 + \frac{1}{A(s)} \right) - \frac{v_o}{A(s)} sC_{gd2} \tag{A.9}$$

$$\Rightarrow v_3 = v_o \frac{-G_m \left(1 + \frac{1}{A(s)} \right) - \frac{sC_{gd2}}{A(s)}}{s(C_{\text{ad,tot}} + C_{gd2}) + \frac{1}{R_o}} \tag{A.10}$$

Rearranging Eq. (A.2) for the voltages gives

$$v_1(sC_{gd1} - g_{m1}) + v_2\left(-s(C_{gd1} + C_{gd2}) - \frac{1}{R_f} - \frac{1}{r_o}\right) + v_3(-g_{m2} + sC_{gd2}) + \frac{v_o}{R_f} = 0 \tag{A.11}$$

Substitution of Eq. (A.6) in Eq. (A.11) yields

$$v_1(sC_{gd1} - g_{m1}) + v_3(-g_{m2} + sC_{gd2}) + v_o\left(\frac{1}{R_f} + \frac{s(C_{gd1} + C_{gd2}) + \frac{1}{R_f} + \frac{1}{r_o}}{A(s)}\right) = 0 \tag{A.12}$$

Substituting Eqs. (A.8) and (A.10) into the preceding equation gives

$$v_i \frac{sC_{\text{mic}}(sC_{gd1} - g_{m1})}{s(C_{\text{mic}} + C_{gd} + C_{gs}) + \frac{1}{r_{\text{in}}}} + v_o\left(\frac{-G_m\left(1 + \frac{1}{A(s)}\right) - \frac{sC_{gd2}}{A(s)}}{sC_{\text{ad,tot}} + \frac{1}{R_o} + sC_{gd2}}(-g_{m2} + sC_{gd2}) \ldots\right.$$
$$\left. \ldots - \frac{\frac{sC_{gd1}}{A}(sC_{gd1} - g_{m1})}{s(C_{\text{mic}} + C_{gd1} + C_{gs1}) + \frac{1}{r_{\text{in}}}} + \frac{1}{R_f} + \frac{s(C_{gd1} + C_{gd2}) + \frac{1}{R_f} + \frac{1}{r_o}}{A(s)}\right) = 0 \tag{A.13}$$

The transfer function of the circuit in the Laplace domain is given by

$$H(s) = \frac{v_o}{v_i} = \frac{-sC_{\text{mic}}(sC_{gd1} - g_{m1})}{\left(s(C_{\text{mic}} + C_{gd1} + C_{gs1}) + \frac{1}{r_{\text{in}}}\right) \cdot \left(\frac{-G_m\left(1+\frac{1}{A(s)}\right) - \frac{sC_{gd2}}{A(s)}}{s(C_{\text{ad,tot}} + C_{gd2}) + \frac{1}{R_o}}(-g_{m2} + sC_{gd2}) \ldots\right.}$$
$$\left. \ldots - \frac{sC_{gd1}A(s)(sC_{gd} - g_{m1})}{s(C_{\text{mic}} + C_{gd1} + C_{gs1}) + \frac{1}{r_{\text{in}}}} + \frac{1}{R_f} + \frac{s(C_{gd1} + C_{gd2}) + \frac{1}{R_f} + \frac{1}{r_o}}{A(s)}\right) \tag{A.14}$$

Simulations with MATLAB have shown (see Fig. A.5) that in the frequency range of interest and for the circuit parameters extracted from T-SPICE the denominator can be simplified to

$$H(s) = \frac{-sC_{\text{mic}}(sC_{gd1} - g_{m1})}{\left(s(C_{\text{mic}} + C_{gd1} + C_{gs1}) + \frac{1}{r_{\text{in}}}\right) \cdot \left(\frac{-G_m\left(1+\frac{1}{A(s)}\right) - \frac{sC_{gd2}}{A(s)}}{s(C_{\text{ad,tot}} + C_{gd2}) + \frac{1}{R_o}}(-g_{m2} + sC_{gd2}) + \frac{1}{R_f}\right)} \tag{A.15}$$

Substituting the gain function of the OpAmp which contains a single pole from Eq. (3.6) in Subsection 3.1.1 of Chapter 3

$$A(s) = \frac{A_{\text{DC,OA}}}{1 - \frac{s}{p_{\text{OA}}}} = \frac{A_{\text{DC,OA}}}{1 + s \cdot \tau_{\text{p,OA}}} \tag{A.16}$$

into the second term of the denominator of Eq. (A.15)

$$T(s) = \left(-G_m \frac{A_{\mathrm{DC,OA}}+1}{A_{\mathrm{DC,OA}}}\left(1+\frac{\tau_{\mathrm{p,OA}}}{\tau_{\mathrm{p,OA}}+1}\right) - \frac{sC_{gd2}}{A_{\mathrm{DC,OA}}}(1+s\tau_{\mathrm{p,OA}})\right)\cdots \\ \cdots(-g_{m2}+sC_{gd2}) + \frac{s(C_{\mathrm{ad,tot}}+C_{gd2})}{R_f} + \frac{1}{R_o R_f} \tag{A.17}$$

Simplifying and rearranging gives

$$T(s) \approx \left(G_m + \frac{s^2 C_{gd2}\tau_{\mathrm{p,OA}}}{A_{\mathrm{DC,OA}}}\right) g_{m2} + \frac{s(C_{\mathrm{ad,tot}}+C_{gd2})}{R_f} \tag{A.18}$$

$$= s^2 \frac{C_{gd2}\tau_{\mathrm{p,OA}} g_{m2}}{A_{\mathrm{DC,OA}}} + s\frac{C_{\mathrm{ad,tot}}+C_{gd2}}{R_f} + g_{m2}G_m \tag{A.19}$$

$$= g_{m2}G_m\left(s^2\frac{C_{gd2}\tau_{\mathrm{p,OA}}}{A_{\mathrm{DC,OA}}G_m} + s\frac{C_{\mathrm{ad,tot}}+C_{gd2}}{R_f g_{m2}G_m}+1\right) \tag{A.20}$$

The polynomial $T(s)$ has two poles p_2, p_3. Assuming that $p_3 \gg p_2$, the following simplification applies

$$T(s) = s^2 a + sb + 1 = \left(1-\frac{s}{p_2}\right)\left(1-\frac{s}{p_3}\right) = s^2\frac{1}{p_2 p_3} - s\left(\frac{1}{p_2}+\frac{1}{p_3}\right)+1 \tag{A.21}$$

$$\overset{p_3 \gg p_2}{\approx} s^2\frac{1}{p_2 p_3} - s\frac{1}{p_2}+1 \tag{A.22}$$

Thus, the poles are given by

$$p_2 = -\frac{1}{b} = -\frac{R_f g_{m2} G_m}{C_{\mathrm{ad,tot}}+C_{gd2}} \tag{A.23}$$

$$p_3 = -\frac{b}{a} = -\frac{A_{\mathrm{DC,OA}}(C_{\mathrm{ad,tot}}+C_{gd2})}{C_{gd2}\tau_{\mathrm{p,OA}} g_{m2} R_f} \tag{A.24}$$

The transfer function in the Laplace domain from the equivalent microphone input voltage v_i to the microphone preamplifier output v_o is

$$H(s) = \frac{g_{m1}C_{\mathrm{mic}}r_{\mathrm{in}}}{g_{m2}G_m R_o}\frac{s\left(s(C_{\mathrm{ad,tot}}+C_{gd2})R_o+1\right)\left(1-s\frac{C_{gd}}{g_{m1}}\right)}{\left(1+s(C_{\mathrm{mic}}+C_{gd1}+C_{gs1})r_{\mathrm{in}}\right)\left(1+s\frac{C_{\mathrm{ad,tot}}+C_{gd2}}{R_f g_{m2}G_m}\right)\cdots} \\ \overline{\cdots\left(1+s\frac{C_{gd2}\tau_{\mathrm{p,OA}}g_{m2}R_f}{A_{\mathrm{DC,OA}}(C_{ad}+C_{gd2})}\right)} \\ = \frac{g_{m1}C_{\mathrm{mic}}r_{\mathrm{in}}}{g_{m2}G_m R_o}\frac{s\left(1-\frac{s}{z_2}\right)\left(1+\frac{s}{z_3}\right)}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)\left(1-\frac{s}{p_3}\right)} \tag{A.25}$$

where

$$z_1 = 0 \tag{A.26}$$

$$z_2 = \frac{1}{(C_{\text{ad,tot}} + C_{gd2})R_o} \tag{A.27}$$

$$z_3 = \frac{g_{m1}}{C_{gd}} \tag{A.28}$$

$$p_1 = -\frac{1}{(C_{\text{mic}} + C_{gd1} + C_{gs1})r_{\text{in}}} \tag{A.29}$$

$$p_2 = -\frac{R_f g_{m2} G_m}{C_{\text{ad,tot}} + C_{gd2}} \tag{A.30}$$

$$p_3 = -\frac{A_{\text{DC,OA}}(C_{\text{ad,tot}} + C_{gd2})}{\tau_{\text{p,OA}} C_{gd2} g_{m2} R_f} = -\frac{\text{GBP}_{\text{OA}}(C_{\text{ad,tot}} + C_{gd2})}{C_{gd2} g_{m2} R_f} \tag{A.31}$$

where GBP_{OA} is the gain-bandwidth product of the OpAmp. Because the transfer function contains both three zeros and three poles and a term causing a high-frequency pole was neglected in Eq. (A.14), the magnitude of the frequency response is flat for high frequencies. Otherwise the system would roll off for infinitely high frequencies.

The pass-band (or in-band) gain is found to be

$$H_{\text{PB}} = \frac{g_{m1} C_{\text{mic}} r_{\text{in}}}{g_{m2} G_m R_o} \frac{|p_1| \cdot |p_2|}{z_2} = g_{m1} R_f \frac{C_{\text{mic}}}{C_{\text{mic}} + C_{gd1} + C_{gs1}} \tag{A.32}$$

The gain-bandwidth product GBP of the microphone preamplifier circuit is given by

$$\text{GBP} = H_{\text{PB}} \cdot |p_3| = \frac{A_{\text{DC,OA}}(C_{\text{ad,tot}} + C_{gd2}) g_{m1} C_{\text{mic}}}{\tau_{\text{p,OA}} C_{gd2} g_{m2} (C_{\text{mic}} + C_{gd1} + C_{gs1})} \tag{A.33}$$

$$= \frac{\text{GBP}_{\text{OA}}(C_{\text{ad,tot}} + C_{gd2}) g_{m1} C_{\text{mic}}}{C_{gd2} g_{m2} (C_{\text{mic}} + C_{gd1} + C_{gs1})} \tag{A.34}$$

A.1.1 Numerical Calculations

The parameters of the circuit elements are extracted from T-Spice and are listed in Table A.1.

OpAmp
$I_{\mathrm{b1,OA}} = 46.8$ nA
$I_{\mathrm{b2,OA}} = 11$ μA
$C_M = 300$ fF
$A_{\mathrm{DC,OA}} = 116.68$ dB
$f_{\mathrm{p,OA}} = 400$ mHz
$\mathrm{GBP_{OA}} = 1.7149$ MHz
$V_{\mathrm{ref}} = 1.3$ V
OTA
$I_{\mathrm{b,OTA}} = 7.69$ pA
$\kappa = 0.7$
$G_m = 105.96$ pS
$R_o = 9.0416 \times 10^{12}$ Ω

JFET
$g_{m1} = 247\mu$S
$g_{ds1} = 15\mu$S
$C_{gs1} = 220$ pF
$C_{gs1} = 160$ pF
pFET
$g_{m2} = 1.24$ mS
$g_{ds2} = 3\mu$S
$C_{gs2} = 415$ fF
$C_{gd2} = 6.57$ pF
$C_{gb2} = 810$ fF

$C_{\mathrm{mic}} = 1$ nF
$r_{\mathrm{in}} = 100$ MΩ
$R_f = 300$ kΩ
$C_{ad} = 10$ pF
$C_{\mathrm{ad,tot}} = 11.225$ pF

Table A.1: (Small-signal) circuit parameters of the microphone preamplifier extracted from T-Spice.

$$f_{z1} = 0 \text{ Hz} \tag{A.35}$$

$$f_{z2} = \frac{z_2}{2\pi} = \frac{1}{2\pi(C_{\mathrm{ad,tot}} + C_{gd2})R_o} = 0.98918 \text{ mHz} \tag{A.36}$$

$$f_{z3} = \frac{z_3}{2\pi} = \frac{g_{m1}}{2\pi C_{gd}} = 245.70 \text{ kHz} \tag{A.37}$$

$$f_{p1} = \frac{|p_1|}{2\pi} = \frac{1}{2\pi(C_{\mathrm{mic}} + C_{gd1} + C_{gs1})r_{\mathrm{in}}} = 1.1533 \text{ Hz} \tag{A.38}$$

$$f_{p2} = \frac{|p_2|}{2\pi} = \frac{R_f g_{m2} G_m}{2\pi(C_{\mathrm{ad,tot}} + C_{gd2})} = 352.5389 \text{ Hz} \tag{A.39}$$

$$f_{p3} = \frac{|p_3|}{2\pi} = \frac{A_{\mathrm{DC,OA}}(C_{\mathrm{ad,tot}} + C_{gd2})}{2\pi\tau_{\mathrm{p,OA}} C_{gd2} g_{m2} R_f} = 1.9872 \text{ kHz} \tag{A.40}$$

$$H_{\mathrm{PB}} = g_{m1} R_f \frac{C_{\mathrm{mic}}}{C_{\mathrm{mic}} + C_{gd1} + C_{gs1}} = 53.6957 = 34.5988 \text{ dB} \tag{A.41}$$

$$\mathrm{GBP} = \frac{\mathrm{GBP_{OA}}(C_{\mathrm{ad,tot}} + C_{gd2}) g_{m1} C_{\mathrm{mic}}}{C_{gd2} g_{m2}(C_{\mathrm{mic}} + C_{gd1} + C_{gs1})} = 670.45 \text{ kHz} \tag{A.42}$$

A.2 Analysis of the Second Pole

The aim of this section is to give a qualitative explanation of the effects causing the second pole p_2, which was analytically derived in the preceding section.

The time constant, which is inversely proportional to the pole frequency, is the product of the equivalent node resistance R_{node} and the equivalent node capacitance

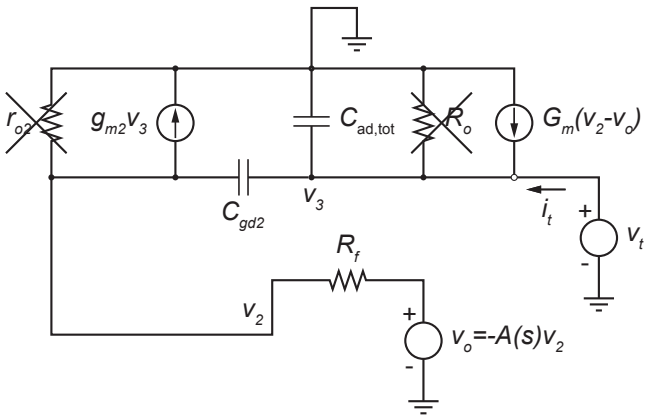


Figure A.2: Circuit for the calculation of the node resistance and capacitance of the adaptive element.

C_{node}

$$\tau_{\text{node}} = R_{\text{node}} \cdot C_{\text{node}} \tag{A.43}$$

The equivalent node resistance of node v_3 can be found by applying a test voltage source v_t at node v_3 and measuring the test current without considering the capacitive effects as shown in Fig. A.2. This way the feedback loop is taken into account. The ratio v_t/i_t is equal to the equivalent resistance R_{eq}. Applying a test voltage v_t creates a small-signal current through the pFET which is equal to $g_{m2} \cdot v_t$. This current is amplified across the feedback resistor R_f and turned into a voltage $v_{R_f} = R_f g_{m2} \cdot v_t$. The voltage drop across the resistor is sensed by the OTA and converted into the final small-signal test current $i_t = G_m R_f g_{m2} \cdot v_t$. Therefore, the associated resistance is given by

$$R_{eq} = \frac{v_t}{i_t} = \frac{1}{G_m R_f g_{m2}} \tag{A.44}$$

The total node resistance is given by the equivalent resistance in parallel with the output resistance of the OTA, which simplifies to R_{eq} because R_{eq} is much smaller than R_o

$$R_{\text{node}} = R_{eq} \parallel R_o \overset{R_{eq} \ll R_o}{\approx} R_{eq} = \frac{1}{G_m R_f g_{m2}} \tag{A.45}$$

Here, the elements of the microphone model are not considered for simplicity. Assuming that the OpAmp has infinite gain and is infinitely fast, it clamps the input of the OpAmp v_2 approximately at virtual ground. The associated node capacitance C_{node} is the capacitance of the adaptive element $C_{\text{ad,tot}}$ in parallel with the parasitic gate-to-drain capacitance C_{gd2} of the pFET

$$C_{\text{node}} = C_{\text{ad,tot}} + C_{gd2} \tag{A.46}$$

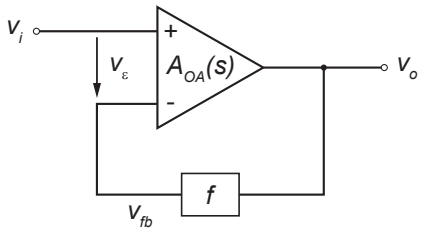


Figure A.3: Operational amplifier in feedback configuration.

Hence, the associated time constant of node v_3 is given by

$$\tau_{\text{node}} = R_{\text{node}} C_{\text{node}} = \frac{C_{ad} + C_{gd2}}{G_m R_f g_{m2}} \tag{A.47}$$

and the pole is given by

$$p_2 = \frac{1}{\tau_{\text{node}}} = \frac{G_m R_f g_{m2}}{C_{ad} + C_{gd2}} \tag{A.48}$$

Thus, the results of the foregoing section are qualitatively explained and confirmed.

A.3 Analysis of the Third Pole

To explain the effects causing the third pole, the influence of feedback on bandwidth needs to be discussed based on [22] (pp. 624–625).

A.3.1 Relation Between Gain and Bandwidth in Feedback Amplifiers

Consider first an OpAmp in feedback configuration as shown in Fig. A.3 with a simple basic amplifier whose gain function contains a single pole

$$A_{\text{OA}}(s) = \frac{A_{\text{DC,OA}}}{1 - \frac{s}{p_{\text{OA}}}} = \frac{A_{\text{DC,OA}}}{1 + s \cdot \tau_{\text{p,OA}}} \tag{A.49}$$

where $A_{\text{DC,OA}}$ is the low-frequency gain of the OpAmp and p_{OA} and $\tau_{\text{p,OA}}$ are the pole and the time constant, respectively. The feedback configuration minimizes the error signal v_ϵ

$$v_\epsilon = v_i - v_{fb} \tag{A.50}$$

The output signal of the OpAmp is equal to

$$v_o = A_{\text{OA}}(s) \cdot v_\epsilon \tag{A.51}$$

where $A_{\mathrm{OA}}(s)$ is the open loop gain of the amplifier. The amount of the output signal which is fed back to the input of the amplifier is given by

$$v_{fb} = f \cdot v_o \tag{A.52}$$

where f is the feedback function. The feedback function f is a positive constant if we assume that the feedback path is purely resistive. This assumption is valid for the feedback configuration in the context of the microphone preamplifier. The overall gain is

$$v_o = A_{\mathrm{OA}}(s) \cdot v_\epsilon = A_{\mathrm{OA}}(s) \cdot (v_i - v_{fb}) = A_{\mathrm{OA}}(s)(v_i - f \cdot v_o) \tag{A.53}$$

$$\Rightarrow \frac{v_o}{v_i} = \frac{A_{\mathrm{OA}}(s)}{1 + A_{\mathrm{OA}}(s) \cdot f} = \frac{A_{\mathrm{OA}}(s)}{1 + T(s)} \tag{A.54}$$

where $T(s) = A_{\mathrm{OA}}(s) \cdot f$ is the loop gain. Substitution of Eq. (A.49) in Eq. (A.54) gives

$$A(s) = \frac{\frac{A_{\mathrm{DC,OA}}}{1-\frac{s}{p_{\mathrm{OA}}}}}{1 + \frac{A_{\mathrm{DC,OA}} f}{1-\frac{s}{p_{\mathrm{OA}}}}} = \frac{A_{\mathrm{DC,OA}}}{1 - \frac{s}{p_{\mathrm{OA}}} + A_{\mathrm{DC,OA}} f} \tag{A.55}$$

$$= \frac{\mathrm{A_{DC,OA}}}{1 + A_{\mathrm{DC,OA}} f} \frac{1}{1 - \frac{s}{p_{\mathrm{OA}}} \frac{1}{1+A_{\mathrm{DC,OA}} f}} \tag{A.56}$$

From Eq. (A.56) the low-frequency gain A_0 is

$$A_0 = \frac{A_{\mathrm{DC,OA}}}{1 + T_0} \tag{A.57}$$

where

$$T_0 = A_{\mathrm{DC,OA}} f \tag{A.58}$$

is the low-frequency loop gain. From Eq. (A.56) the cutoff frequency (i.e. the new pole magnitude) and the time constant of the feedback circuit are

$$p = (1 + A_{\mathrm{DC,OA}} f) \cdot |p_{\mathrm{OA}}| = \frac{1 + A_{\mathrm{DC,OA}} f}{\tau_{\mathrm{p,OA}}} \tag{A.59}$$

$$\tau = \frac{1}{1 + A_{\mathrm{DC,OA}} f} \tau_{\mathrm{p,OA}} \tag{A.60}$$

Thus the feedback has reduced the low-frequency gain by a factor $(1 + T_0)$ but the cutoff frequency has been increased by the same amount $(1 + T_0)$. Note that the gain-bandwidth product (GBP) is constant

$$\mathrm{GBP} = A_{\mathrm{DC,OA}} \cdot p_{\mathrm{OA}} = \frac{A_{\mathrm{DC,OA}}}{\tau_{\mathrm{p,OA}}} \tag{A.61}$$

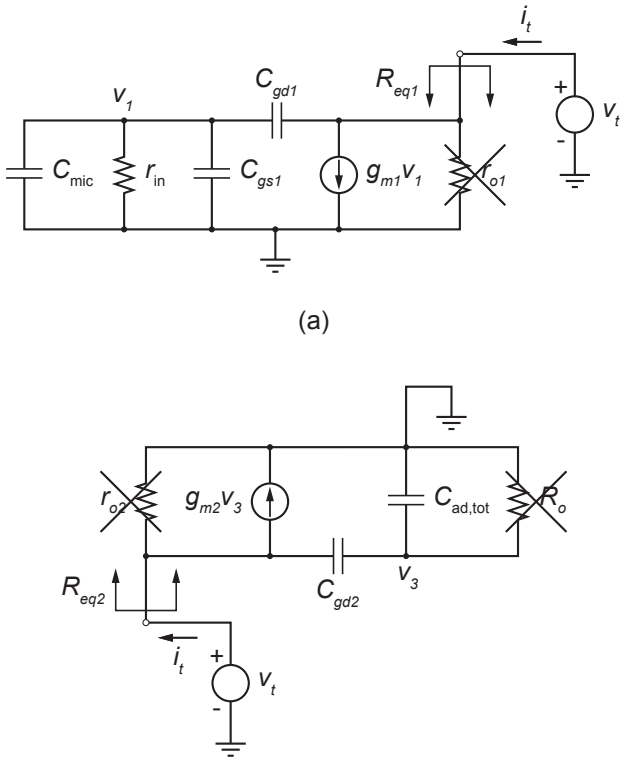


Figure A.4: (a) Circuit for the calculation of the equivalent resistance looking into the microphone model. Note that the equivalent microphone voltage source is shorted. (b) Circuit for the calculation of the equivalent resistance looking into the pFET of the adaptive element.

A.3.2 Determination of the Feedback Function

In this subsection the feedback function, which alters the bandwidth of the feedback circuit, is derived. The total equivalent resistance R_{eq} which forms a voltage divider together with the feedback resistor of the OpAmp is determined by the equivalent resistance R_{eq1} looking into the microphone model in parallel with the equivalent resistance R_{eq2} looking into the pFET of the adaptive element.

A test voltage source v_t is applied at the output of the microphone model to measure the test current and to determine the equivalent resistance while the input

voltage source v_i is shorted as shown in Fig. A.4 (a)

$$v_1 = \frac{\frac{1}{s(C_{\text{mic}}+C_{gs1})+\frac{1}{r_{\text{in}}}}}{\frac{1}{sC_{gd1}}+\frac{1}{s(C_{\text{mic}}+C_{gs1})+\frac{1}{r_{\text{in}}}}} v_t = \frac{sC_{gd1}}{s(C_{\text{mic}}+C_{gs1}+C_{gd1})+\frac{1}{r_{\text{in}}}} v_t \tag{A.62}$$

$$\approx \frac{C_{gd1}}{C_{\text{mic}}+C_{gs1}+C_{gd1}} v_t = \frac{1}{1+\frac{C_{\text{mic}}+C_{gs1}}{C_{gd1}}} \approx \frac{1}{8} v_t \tag{A.63}$$

In both analyses the output resistances of the pFET and JFET are neglected because they are much higher. Moreover, the currents through the capacitive dividers are not considered. The input test current is

$$i_t \approx g_{m1} v_1 = \frac{g_{m1}}{1+\frac{C_{\text{mic}}+C_{gs1}}{C_{gd1}}} v_t \tag{A.64}$$

The equivalent resistance R_{eq1} is given by

$$R_{eq1} = \frac{v_t}{i_t} = \frac{1+\frac{C_{\text{mic}}+C_{gs1}}{C_{gd1}}}{g_{m1}} = 34.919\ \text{k}\Omega \tag{A.65}$$

Similarly, the equivalent resistance looking into the drain of the pFET of the adaptive element can be determined (see Fig. A.4 (b))

$$i_t = g_{m2}\frac{C_{gd2}}{C_{\text{ad,tot}}+C_{gd2}} v_t + \frac{sC_{\text{ad,tot}}C_{gd2}}{C_{ad}+C_{gd2}} v_t \tag{A.66}$$

$$\approx g_{m2}\frac{C_{gd2}}{C_{\text{ad,tot}}+C_{gd2}} v_t \tag{A.67}$$

The equivalent resistance R_{eq2} is

$$R_{eq2} = \frac{v_t}{i_t} = \frac{C_{\text{ad,tot}}+C_{gd2}}{g_{m2}C_{gd2}} = 2.1843\ \text{k}\Omega \tag{A.68}$$

which is much smaller by a factor of 15 than the input resistance seen looking into the pFET and the adaptive element. We assume that feedback through the OTA has no effect because it forms a low-pass filter and high frequencies are attenuated. Therefore, the total resistance is found to be

$$R_{eq} = R_{eq1} \parallel R_{eq2} \overset{R_{eq1} \gg R_{eq2}}{\approx} R_{eq2} \tag{A.69}$$

The voltage divider rule from the output of the OpAmp v_0 to the inverting input v_2 yields

$$v_2 = \frac{R_{eq}}{R_{eq}+R_f} v_0 \overset{R_f \gg R_{eq}}{\approx} \frac{R_{eq}}{R_f} v_0 = \frac{C_{\text{ad,tot}}+C_{gd2}}{C_{gd2}g_{m2}R_f} v_o \tag{A.70}$$

The feedback function is given by

$$f = \frac{v_2}{v_0} = \frac{C_{gd2} + C_{\text{ad,tot}}}{C_{gd2} g_{m2} R_f} \tag{A.71}$$

From Eq. (A.59) the magnitude of the pole is

$$|p_3| = (1 + A_{\text{DC,OA}} f) \cdot p_{\text{OA}} \overset{A_{\text{DC,OA}} f \gg 1}{\approx} A_{\text{DC,OA}} f \cdot p_{\text{OA}} = \frac{A_{\text{DC,OA}} f}{\tau_{\text{p,OA}}} \tag{A.72}$$

$$= \frac{A_{\text{DC,OA}} (C_{\text{ad,tot}} + C_{gd2})}{\tau_{\text{p,OA}} C_{gd2} g_{m2} R_f} = \frac{\text{GBP}_{\text{OA}} (C_{\text{ad,tot}} + C_{gd2})}{C_{gd2} g_{m2} R_f} \tag{A.73}$$

which is in accordance with the results obtained in Section A.1. It is apparent that the magnitude of the third pole $|p_3|$ is proportional to the gain-bandwidth product of the OpAmp GBP_{OA} and inversely proportional to the capacitive divider ratio.

A.4 Discussion of the Results

It is shown that the pole causing the rolloff in the transfer function of the microphone preamplifier is caused by capacitive coupling from the OpAmp onto the gate of the pFET through C_{gd2} and that the bandwidth is drastically reduced.

Theoretically, the gain-bandwidth product of the OpAmp GBP_{OA} can be reduced to move the third pole to lower frequencies by decreasing the bias current of the output stage of the OpAmp. However, this current cannot be further reduced in the present design because the bias current should be capable of delivering at least the maximum signal current of the microphone in the order of 10 μA. Otherwise the OpAmp slews and the signal is clipped.

Alternatively, the frequency of the third pole can be lowered by making the pFET of the adaptive element M_2 wider which in turn increases its parasitic gate-to-drain capacitance C_{gd2} or by deliberately connecting a capacitor between the gate and the drain of the pFET to increase the effective gate-to-drain capacitance.

For the simplified analysis in Subsection 3.1.4 of Chapter 3, the feedback function f was equal to 1 because the parasitic capacitances and output resistances of the pFET and the JFET were not considered and the equivalent resistance $R_{eq} \to \infty$.

$$f = \frac{R_{eq}}{R_{eq} + R_f} \overset{R_{eq} \to \infty}{\to} 1 \tag{A.74}$$

Therefore, the bandwidth of the circuit was maximum.

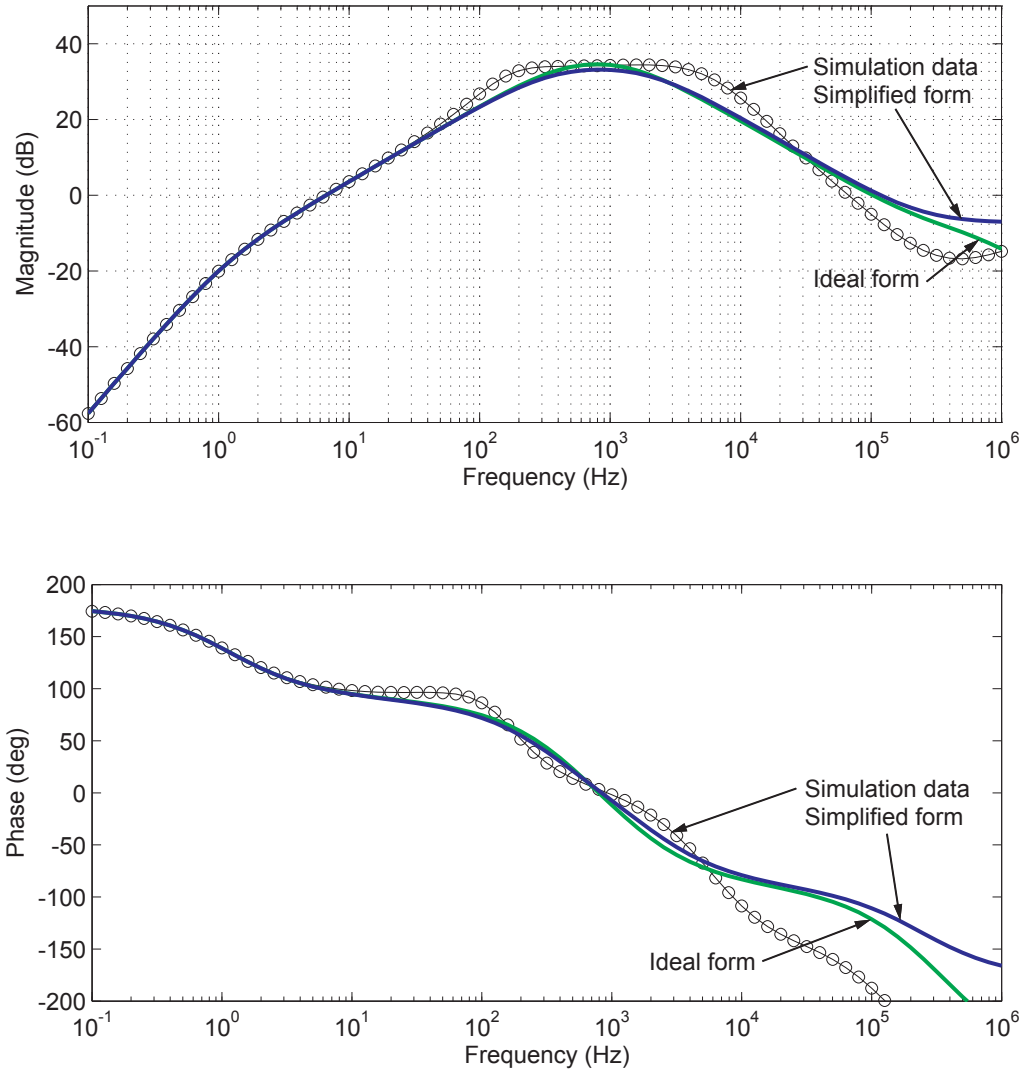


Figure A.5: Transfer function of the microphone preamplifier including the microphone model from the microphone equivalent voltage source to the preamplifier output voltage. The ideal form includes the terms which are neglected in order to derive the poles determining the pass-band. It is apparent that the terms influence the frequency response only for high frequencies and that the approximation is appropriate for the derivation of the poles p_2 and p_3.

Appendix B

Details Required for Chip Testing

Cochlea subversion base URL:
https://svn.ini.unizh.ch/repos/avlsi/common/projects/cochleaAMSBiasgenPreamp
(password protected)

Dollbrain project subversion base URL:
https://svn.ini.uzh.ch/repos/avlsi/db (password protected)

Bibliography

[1] DollBrain project: Micropower integrated face and voice detection. Available: http://dollbrain.ini.uzh.ch.

[2] M. C. Büchler. *Algorithms for Sound Classification in Hearing Instruments.* Diss. ETH no 14498, 2002.

[3] M. W. Baker and R. Sarpeshkar. "A low-power high-PSRR current-mode microphone preamplifier," *IEEE Journal of Solid-State Circuits*, Vol. 38, Issue 10, pp. 1671–1678, October 2003.

[4] HandiWorks web page. Available: http://www.handiworks.com/pd_find.cfm.

[5] K. Heutschi. *Skript Akustik II (227-0478-00).* Institut für Signal- und Informationsverarbeitung, ETHZ, June 2006.

[6] J. Eargle. *The microphone book.* Elsevier, Amsterdam, 2004.

[7] G. M. Sessler. "Electrostatic Microphones with Electret Foil," *The Journal of the Acoustical Society of America*, Vol. 35, Number 9, pp. 1354–1357, September 1963.

[8] A. van Rhijn. "Integrated Circuits for High Performance Electret Microphones," *Audio Engineering Society Convention Paper*, Amsterdam, March 2003.

[9] Unpublished. Tanner EDA T-Spice 12 User Guide.

[10] Knowles Acoustics MD9745APA-1 data sheet. Available: http://www.farnell.com/datasheets/87224.pdf.

[11] S.-C. Liu, J. Kramer, G. Indivieri, T. Delbruck, and R. Douglas. *Analog VLSI: Circuits and Principles.* MIT Press, Cambridge, November 2002.

[12] T. Delbruck. ""Bump" circuits for computing similarity and dissimilarity of analog voltages," *Proceedings of International Joint Conference on Neural Networks*, Seattle Washington, pp. I–475–479, July 1991.

[13] T. Delbruck and D. Oberhof. "Self biased low power adaptive photoreceptor", *2004 International Symposium on Circuits and Systems (ISCAS 2004)*, Vancouver, pp. IV–844–847, May 2004.

[14] J. Mulder, W. A. Serdijn, A. C. Van der Woerd, and A. H. M. van Roermund. *Dynamic Translinear and Log-Domain Circuits: Analysis and Synthesis.* Kluwer, Boston, 1998.

[15] T. Delbruck and C. A. Mead. "Analog VLSI phototransduction by continuous-time, adaptive, logarithmic photoreceptor circuits," *Vision Chips: Implementing vision algorithms with analog VLSI circuits*, C. Koch and H. Li editors, IEEE Computer Society Press, pp. 139–161, 1995.

[16] S. M. Zhak, M. W. Baker, and R. Sarpeshkar. "A low-power wide dynamic range envelope detector," *IEEE Journal of Solid-State Circuits*, Vol. 38, Issue 10, pp. 1750–1753, October 2003.

[17] M. Baker, S. Zhak, and R. Sarpheshkar. "A micropower envelope detector for audio applications," *Proceedings of the 2003 International Symposium on Circuits and Systems (ISCAS 2003)*, Vol. 5, pp. V–1–4, May 2003.

[18] G. Indiveri, E. Chicca, and R. Douglas. "A VLSI array of low-power spiking neurons and bistable synapses with spiketiming dependent plasticity," *IEEE Transactions on Neural Networks*, Vol. 17, Issue 1, pp. 211–221, January 2006.

[19] D. D. Ben Dayan Rubin, E. Chicca, and G. Indiveri. "Characterizing the firing proprieties of an adaptive analog VLSI neuron," *Lecture Notes in Computer Science*, 3141, pp. 189–200, 2004.

[20] T. Delbruck and A. van Schaik. "Bias current generators with wide dynamic range," *Analog Integrated Circuits and Signal Processing*, Vol. 43, pp. 247–268, 2005.

[21] Unpublished. Maher Kayal. *EDATP Addendum: Guidelines to do an Analog Layout*, Analog IC Design Course, EPFL, 2007.

[22] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer. *Analysis and design of analog integrated circuits.* Fourth edition, Wiley, New York, 2001.