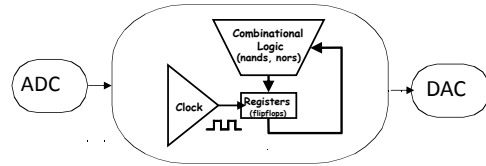


Digital computation

Logic design with FPGAs

- Synchronous logic and logic synthesis
- BASYS2 FPGA board
- Spartan FPGA
- Xilinx ISE WebPACK
- Verilog & Gateway "HelloWorld" exercise

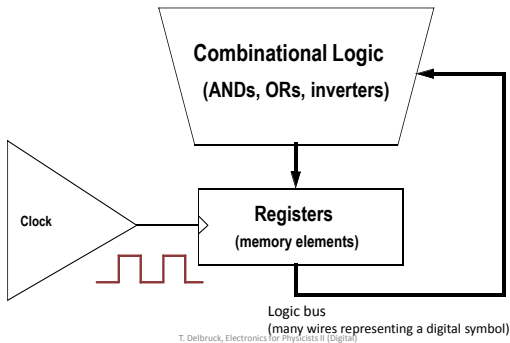


1. Fast global clock
2. Bit-perfect deterministic logical state

T. Delbruck, Electronics for Physicists II (Digital)

T. Delbruck, Electronics for Physicists II (Digital)

Synchronous logic



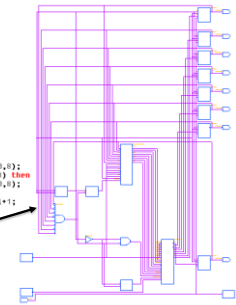
T. Delbruck, Electronics for Physicists II (Digital)

How logic is designed now

Hardware Description Language (VHDL syntax used here)

```
architecture example_arch of example is
    signal CountInternal: unsigned(4,0);
    attribute snc_set_reset of reset: signal is "true";
begin
    process(clock)
    begin
        if rising_edge(clock) then
            if reset='1' then
                CountInternal<=to_unsigned(0,0);
            elsif CountInternal.to_unsigned(4,0) then
                CountInternal<=to_unsigned(0,0);
            else
                CountInternal<=CountInternal+1;
            end if;
        end process;
        count<=CountInternal;
    end example_arch;
```

Logic synthesis



By using HDLs, industry can design complex chips with >100 million logic elements

T. Delbruck, Electronics for Physicists II (Digital)

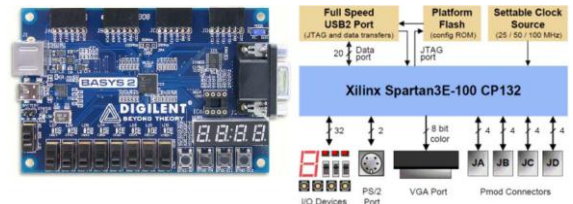
Field Programmable Gate Arrays (FPGAs)

- Reconfigurable logic chips with lots of registers, compared with CPLDs and PALs.
- Range in price from \$10 to \$10,000 per chip depending on number of "gate equivalents".
- They **do not** provide you a processor with instructions, ALU and memory (although you can embed a processor in a larger FPGA).
- Sold by Xilinx, Altera, Lattice, Actel, etc

CPLD = Complex Programmable Logic Device
 PAL = Programmable Array Logic

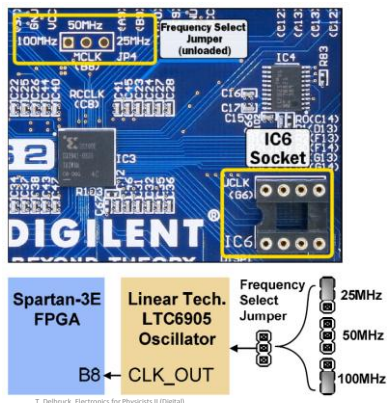
T. Delbruck, Electronics for Physicists II (Digital)

BASYS2 FPGA board Xilinx Spartan 3E XCS100E

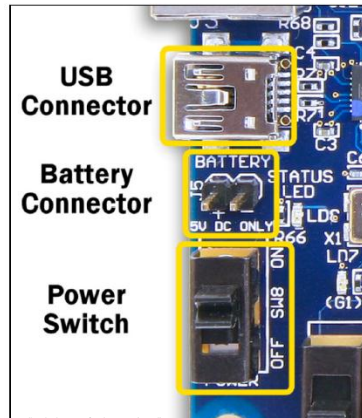


T. Delbruck, Electronics for Physicists II (Digital)

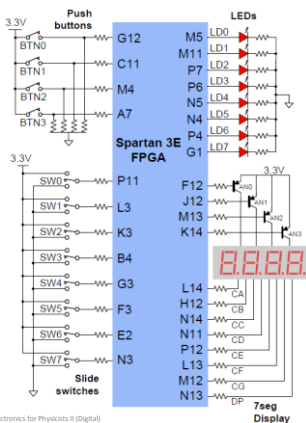
BASYS2 oscillator



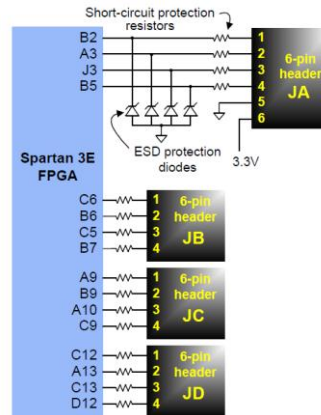
BASYS2 power



BASYS2 IO



BASYS2 PMOD connectors



Digilent external modules (PMODs)

Products Support Classroom Services Showcase About Us My Cart

PmodWiFi - 802.11b/g/n WiFi Interface \$59.99

- IEEE 802.11-compliant RF transceiver
- Serialized unique MAC address
- 1 and 2Mbps data rates
- IEEE 802.11b/g/n-compatible
- Integrated PCB antenna
- Range: up to 400m (1300 ft.)
- Radio regulation certification for the United States (FCC), Canada (IC), Europe (ETSI), and Japan (ARIB)
- Wi-Fi certified (WPA2, WPA2-PSK)
- Ships with a UART crossover cable, a 6" 12-pin cable, a 6" 2x6-pin to dual 6-pin cable, one 12-pin header, and two 6-pin headers

PmodBT - Bluetooth Interface \$54.99

- Provides Bluetooth support in either a transparent serial cable replacement mode or a more powerful command mode
- Wide range of profiles including generic access profile, service discovery profile, and the serial port profile
- Simple UART interface
- 2.5V - 3.0V operating voltage
- Small size (1.6" x 1.5")
- Ships with a UART crossover cable, a 6" 12-pin cable, a 6" 2x6-pin to dual 6-pin cable, one 12-pin header, and two 6-pin headers

PmodNIC - Network Interface Controller \$29.99

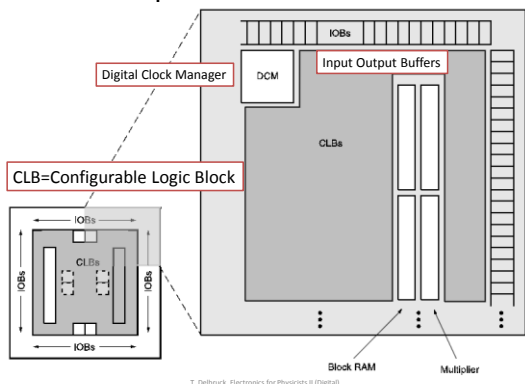
- 10 Mbps IEEE 802.3 compatible Ethernet controller
- SP1 interface
- 10BASE-T MACPHY
- Small size (1.65" x 0.80")
- Ships with a 6" 12-pin cable, a 6" 2x6-pin to dual 6-pin cable, one 12-pin header, and two 6-pin headers

T. Debnick, Electronics for Physicists II (Digital)

BASYS2 capabilities

- Xilinx Spartan 3-E FPGA, 100K or 250K gate
 - FPGA features 18-bit multipliers, 72Kbits of fast dual-port block RAM, and 500MHz+ operation
 - USB 2 full-speed port for FPGA configuration and data transfers (using Adept 2.0 software available as a free download)
 - XCF02 Platform Flash ROM that stores FPGA configurations indefinitely
 - User-settable oscillator frequency (25, 50, and 100 MHz), plus socket for a second oscillator
 - Three on-board voltage regulators (1.2V, 2.5V, and 3.3V) that allow use of 3.5V-5.5V external supplies
 - 8 LEDs, 4-digit seven-segment display, four pushbuttons, 8 slide switches, PS/2 port, and a 8-bit VGA port
 - Four 6-pin headers for user I/Os, and attaching Digilent PMOD accessory circuit boards
- T. Debnick, Electronics for Physicists II (Digital)

Spartan architecture



T. Delbruck, Electronics for Physicists II (Digital)

Spartan 3 XC3S100E

Table 2: Available User I/Os and Differential (Diff) I/O Pairs

Package	VQ100 VQG100		CP132 CPG132		TQ144 TQG144		PQ208 PQG208	
Size (mm)	16 x 16		8 x 8		22 x 22		28 x 28	
Device	User	Diff	User	Diff	User	Diff	User	Diff
XC3S100E	66 (7)	30 (2)	83 (11)	35 (2)	108 (28)	40 (4)	-	-

T. Delbruck, Electronics for Physicists II (Digital)

Device datasheet (233 pages...)



Spartan-3E FPGA Family: Data Sheet

DS312 (v3.8) August 26, 2009

Product Specification

Module 1: Spartan-3E FPGA Family: Introduction and Ordering Information

DS312-1 (v3.8) August 26, 2009

- Introduction
- Features
- Architectural Overview
- Package Marking
- Ordering Information

Module 2: Functional Description

DS312-2 (v3.8) August 26, 2009

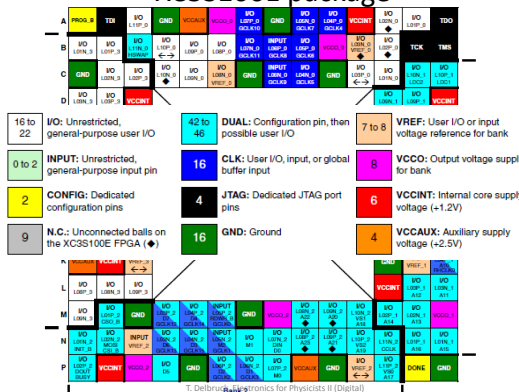
Module 3: DC and Switching Characteristics

DS312-3 (v3.8) August 26, 2009

- DC Electrical Characteristics
 - Absolute Maximum Ratings
 - Supply Voltage Specifications
 - Recommended Operating Conditions
 - DC Characteristics
- Switching Characteristics
 - I/O Timing
 - SLICE Timing
 - DCM Timing
 - Block RAM Timing
 - Multiplier Timing

T. Delbruck, Electronics for Physicists II (Digital)

XC3S100E package



T. Delbruck, Electronics for Physicists II (Digital)

CLBs (Config. Logic Blocks)

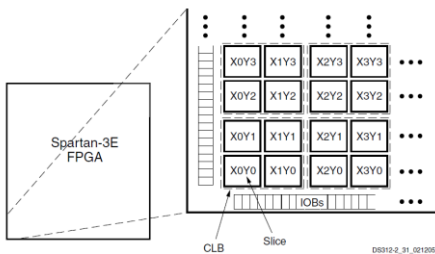


Figure 14: CLB Locations

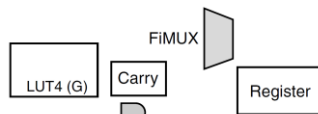
Table 9: Spartan-3E CLB Resources

Device	CLB Rows	CLB Columns	CLB Total ⁽¹⁾	Slices	LUTs / Flip-Flops	Equivalent Logic Cells	RAM16 / SRL16	Distributed RAM Bits
XC3S100E	22	16	240	960	1,920	2,160	960	15,360

T. Delbruck, Electronics for Physicists II (Digital)

CLB structure

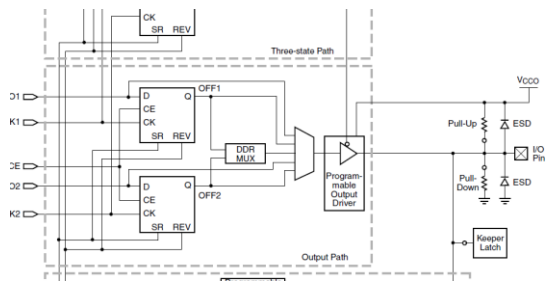
- Each CLB has 4 slices
- Each slice has 4-input LUT (look-up table) logic block and single bit latch (register), plus multiplexors, shift registers, carry bits, RAM, etc.
- One slice simplified: The LUT is programmed to compute any desired logic function of 4 inputs.



- Generally you don't need to know about this; just to be aware of what fabric your synthesized logic is finally mapped to.

T. Delbruck, Electronics for Physicists II (Digital)

Spartan IOB structure (part) (Input Output Buffer)



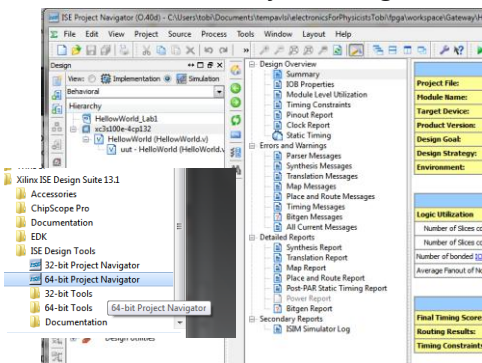
T. Delbruck, Electronics for Physicists II (Digital)

“Gateway” lab exercises

- HelloWorld_Lab1
- HelloLotsOfWorlds_Lab2
- HelloWorldSynchronous_Lab3
- ShiftingTheWorld_Lab4
- ShiftingManyWorlds_Lab5
- CountingTheWorld_Lab6
- TimingTheWorld_Lab7
- DecodingTheWorld_Lab8
- CountingInDecimal_Lab9
- ColouringTheWorld_Lab10
- WorldOfStateMachines_Lab11
- LinkedStateMachine_Lab12

T. Delbruck, Electronics for Physicists II (Digital)

Xilinx ISE Project Navigator



T. Delbruck, Electronics for Physicists II (Digital)

HelloWorld.v

verilog hardware description language (HDL)

```

module HelloWorld(
    input IN,
    output OUT
);

    assign OUT = IN;

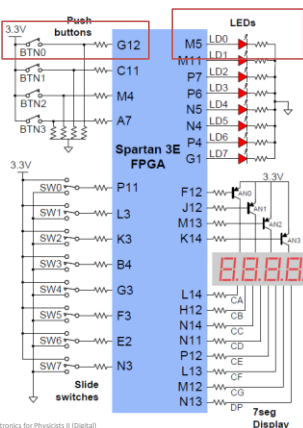
endmodule
    
```

T. Delbruck, Electronics for Physicists II (Digital)

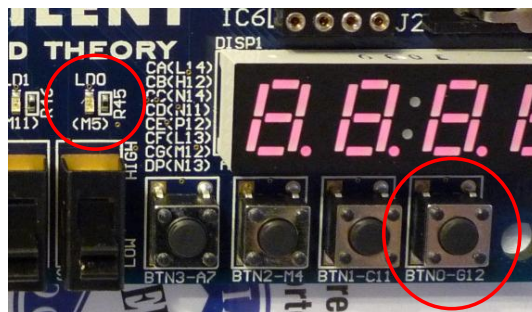
HelloWorld.ucf User Constraints File (UCF)

```

NET "IN" LOC = G12;
// IN connects to pin G12
NET "OUT" LOC = M5;
// OUT to M5
    
```



T. Delbruck, Electronics for Physicists II (Digital)



T. Delbruck, Electronics for Physicists II (Digital)