

Tutorial on neuromorphic engineering
 Part 1: Motivation, history, community
 Part 2: Vision circuits and chips
 Part 3: Hands-on work

Tobi Delbruck
 Inst. of Neuroinformatics
 UZH-ETH Zurich

Hands-on work

Components available


- 3x Tmpdiff128 silicon retinas with USB2 interface
- 1x Tmpdiff128 Stereo board with USB2 interface
- 1x Physiologist's Friend chip
- 2x Servo controller with USB1 interface
- 1x Stocker Optical Flow Sensor with USB1 interface

Hands-on project/discussion ideas

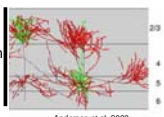
- Plotting receptive fields of retinal and cortical cells using PhysioFriend chip
- Measuring photoreceptor responses and observing membrane voltage of spiking neuron using PhysioFriend
- Building a "Bill Catcher" robot using silicon retina, jAER, and a servo
- Discussing bias generator design

Part 1: Motivation, history,
 community

Computer vs. Brain



Pentium 4




Cortex
1mm

Anderson et al. 2003

At the system level, brains are about 1 million times more power efficient than computers. Why?
 Cost of elementary operation (turning on transistor or synapse) is about the same.
 It's not some magic about physics.

Computer	Brain
Fast global clock	Self-timed
Bit-perfect deterministic logical state	Synapses are stochastic! Computation dances: digital→analog→digital
Memory distant to computation	Memory at computation
Fast high precision power hungry ADCs	Low precision adaptive data-driven quantizers
Devices frozen on fabrication	Constant adaptation and self-modification

The World of Neuromorphic Engineering 2007



www.ethz.ch/neuromorphic

Shih-Chii Liu

Types of Neuromorphic chips

- Silicon retinas—electronic models of retinas
- Silicon cochleas—electronic models of cochleas
- Smart vision chips (e.g. tracking chips, motion sensors, presence sensors)
- Neural networks of spiking neurons
- Central pattern generators
- Models of specific systems:
 e.g. bat sonar echolocation, lamprey spinal cord for swimming, lobster stomatogastric ganglion, electric fishes
- Multichip systems that use spikes for interchip communication

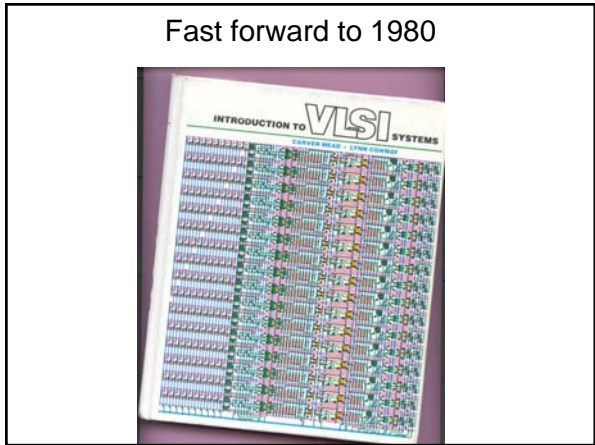
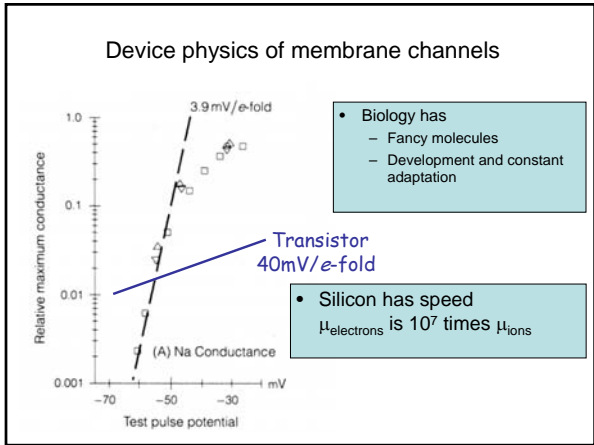
Brief history of neuromorphic engineering

1967-1972 – “The subterranean group”
 Biophysics of membrane channels

Carver Mead (Caltech) Max Delbruck (Caltech)

Moshe Eisenberg (from UPenn)
 Jim Hall (recalled early from Vietnam)
 Peter Leuger (Konstanz)
 Fred Sigworth

Paul Mueller (UPenn)



Physics of Computation Course

1982

1985

Carver Mead

Dick Feynman

John Hopfield

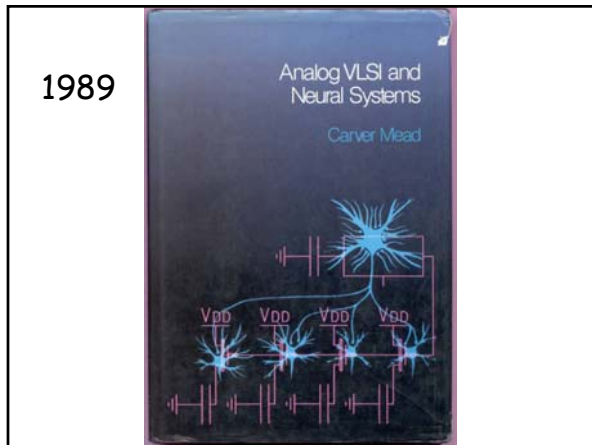
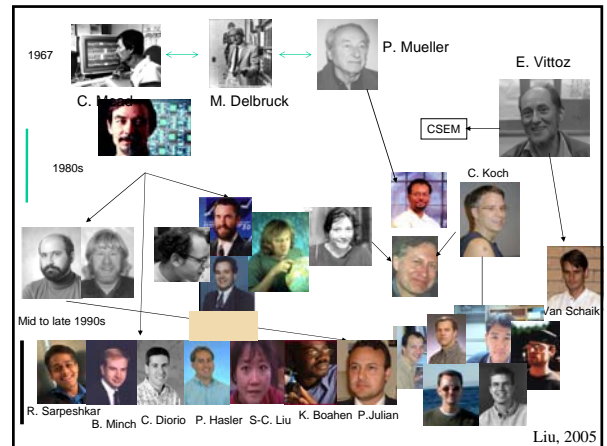
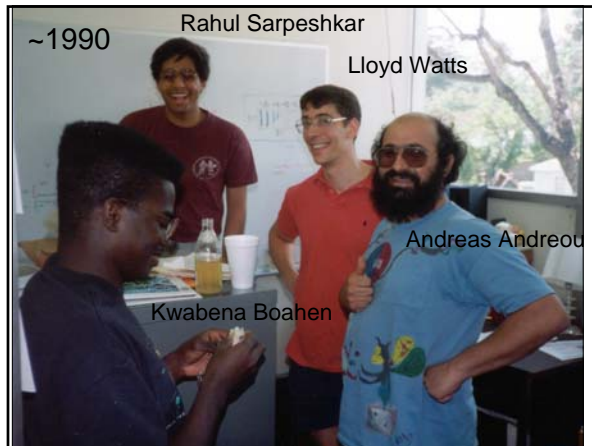
History of Neuromorphic Engineering

The silicon retina, and all that

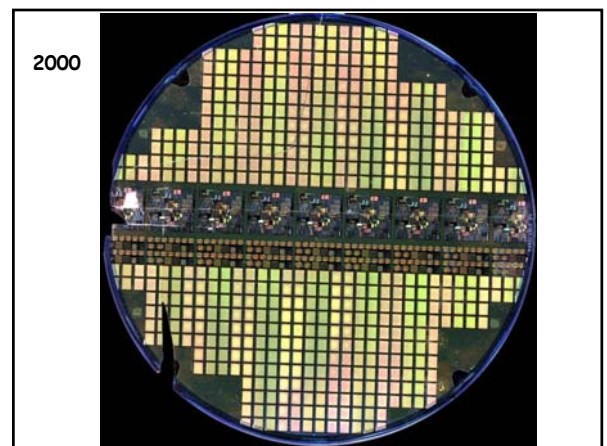
1980s

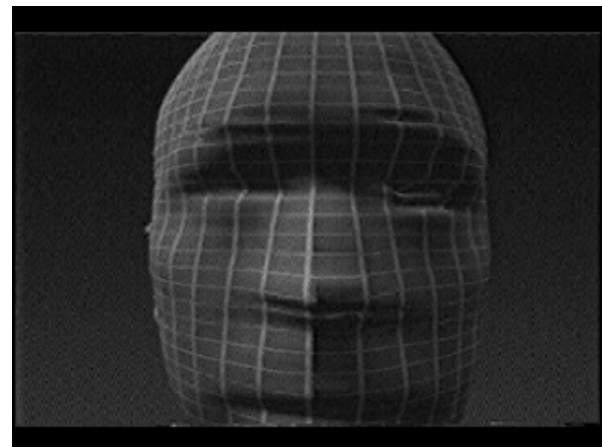
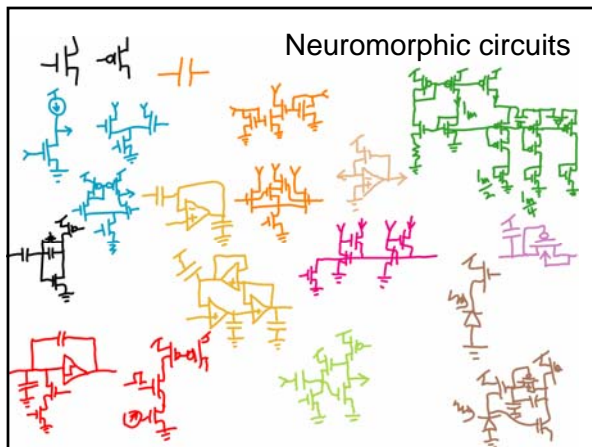
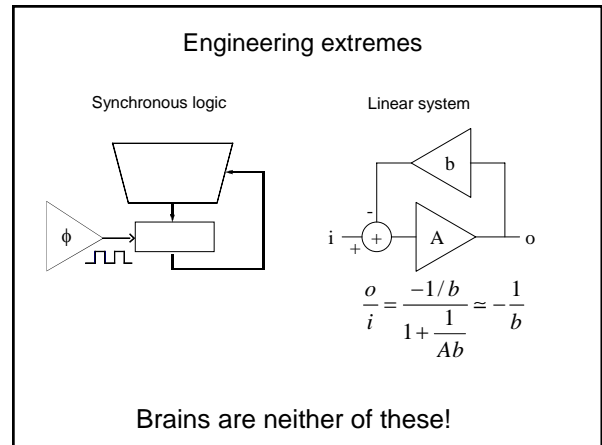
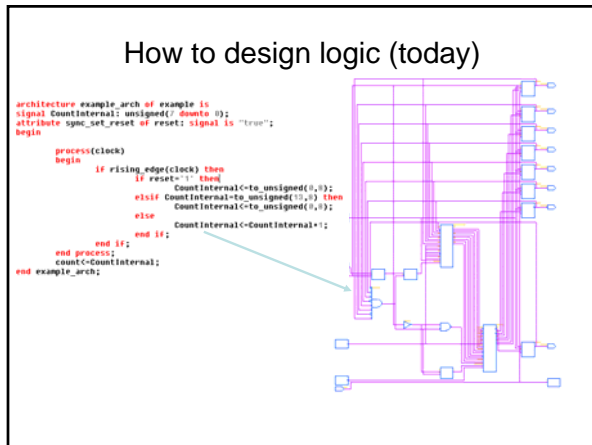
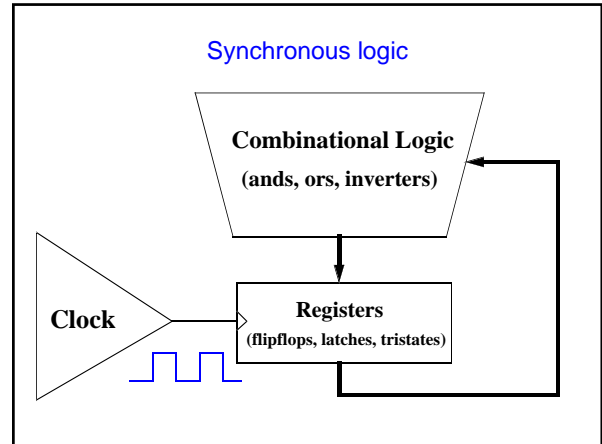
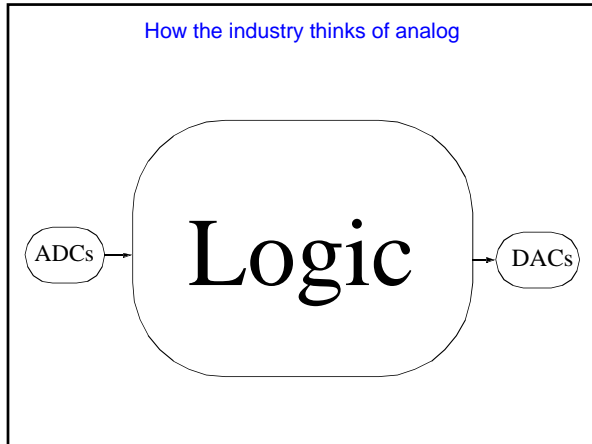
Carver Mead

Misha Mahowald



The motivation for neuromorphic engineering





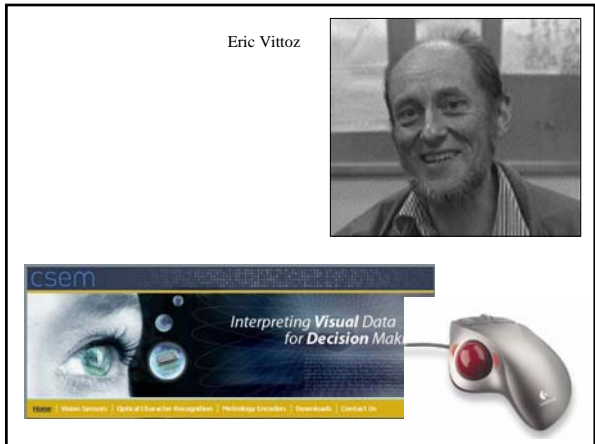
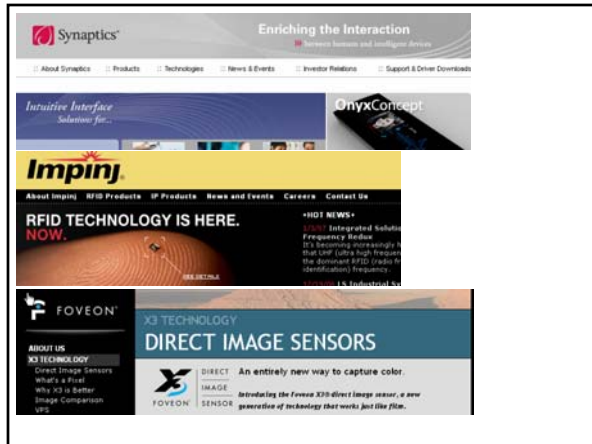
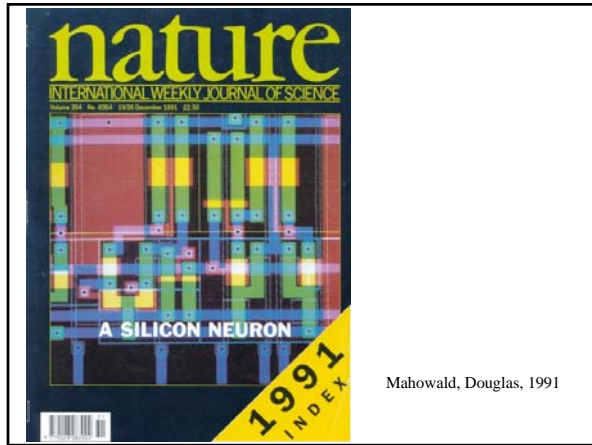
**IF WE ARE TO AVOID THE AI TRAP
 WE HAD BETTER EVOLVE OUR SYSTEMS
 WITH REAL INPUT DATA
 (BOTTOM UP)**

THE AI TRAP:

1. ANNOUNCE INTENTION TO SOLVE AN OBVIOUSLY DIFFICULT PROBLEM
2. WORK LONG ENOUGH TO LEARN THAT IT IS MUCH MORE DIFFICULT THAN WAS INITIALLY SUPPOSED
3. FIND A TOY EXAMPLE THAT CONTAINS ONLY THE EASY PARTS OF THE PROBLEM
4. MAKE DEMO OF TOY EXAMPLE
5. DECLARE THE PROBLEM SOLVED WITHOUT REVEALING WHAT HAS BEEN LEARNED ABOUT THE HARD PARTS
6. GO TO STEP 3. OF A MORE DIFFICULT PROBLEM

Mead ca. 1990

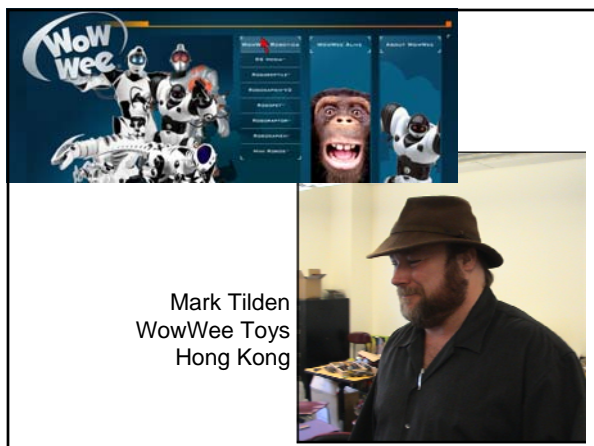
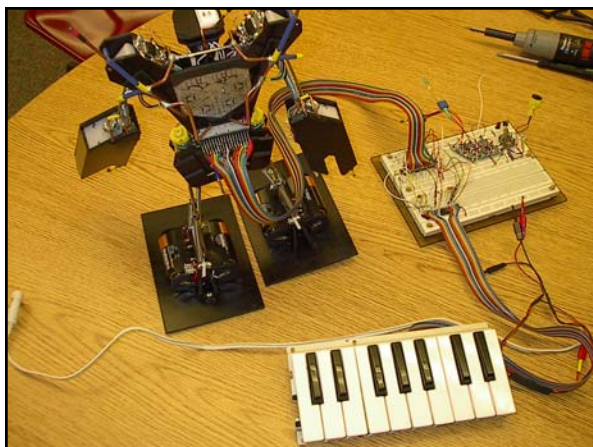
Accomplishments of neuromorphic engineering





What is the Telluride Workshop on Neuromorphic Engineering?

- Focus is on
 - fostering the neuromorphic community,
 - tutorials, hands-on workgroups,
 - establishing long-lasting collaborations
- Running 12 years now, started by Rodney Douglas and Misha Mahowald
- Funded by NSF & others, steadily at about \$110k/yr
- 60 people each year, about half invited and half applicants – **you can apply**. Housing and part of travel is covered.
- 3 weeks long each July, in the mountains in Colorado, USA.
- Google "Telluride Neuromorphic" for more info





- ### 2007 Workgroups
- Workgroups
 - Vision Systems
 - Audition
 - jAER Project: Algorithmic Event-based Computation
 - Spike-based computation and learning with neuromorphic VLSI chips
 - Relational networks of neuromorphic VLSI chips
 - NeuroClone
 - USB Bootcamp
 - Locomotion and Robotics
 - Bias Generators
 - Toy Hacking
 - Analog VLSI Tutorial
 - Design and Test Asynchronous Circuits
 - SMD Soldering Tutorial
 - Using SubVersion for projects
 - Floating Gate Tutorial
 - 3D Animation (Blender)
 - Moth-Machine Interfacing
 - Discussion Groups
 - AER Standards Specifications
 - Non-Technical Stuff
 - T-Shirt Contest
 - Skits
 - Poker
 - Volleyball
 - Tennis
 - Soccer
 - Flyfishing
 - Paragliding
 - Mountain Biking
 - Workshop Photographers

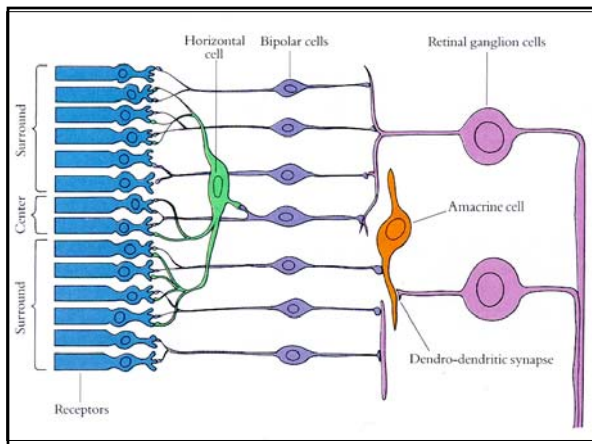
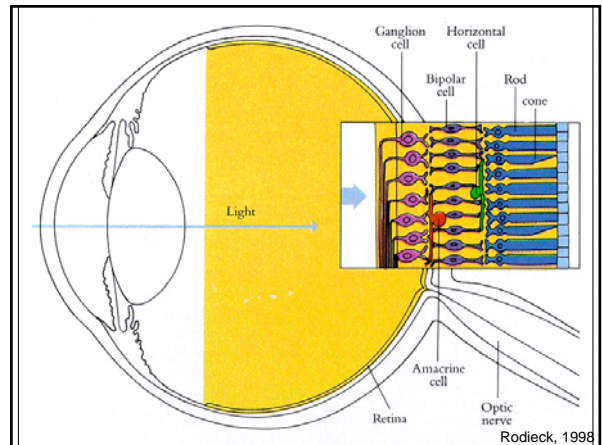
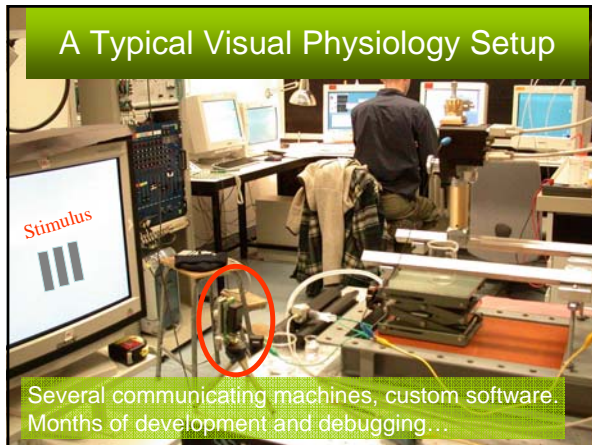
Part 2: Vision circuits and chips

Types of neuromorphic vision sensors

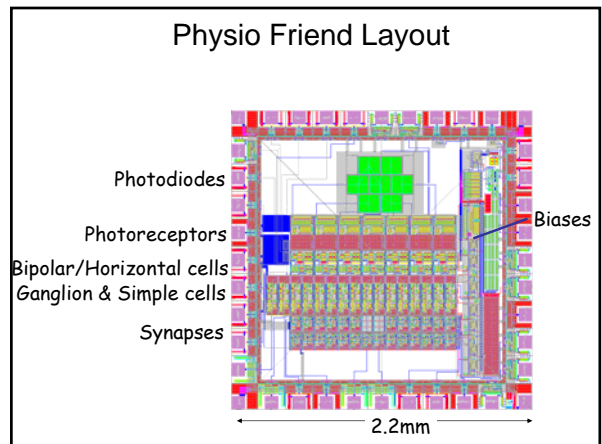
- Silicon retinas as models of biology
- Spike-based sensors for applications
- Motion sensors (many varieties)
- Specialized sensors (activity, tracking)
- Computation-On-Readout (COR) architectures
- Pattern extraction sensors
- Cellular Neural Network (CNN) focal plane processors
- Others: e.g. SeeHear, optical mice, torque sensor, character recognition, check reader

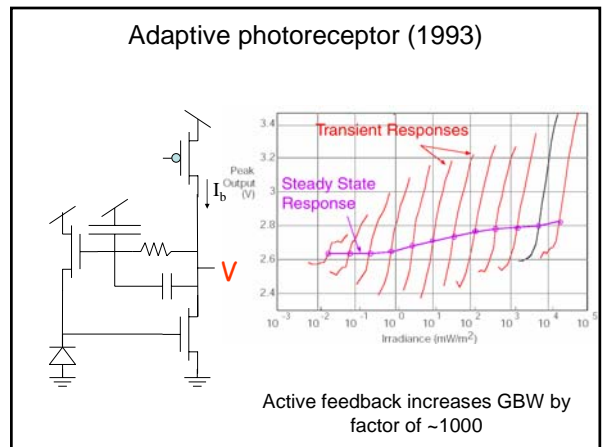
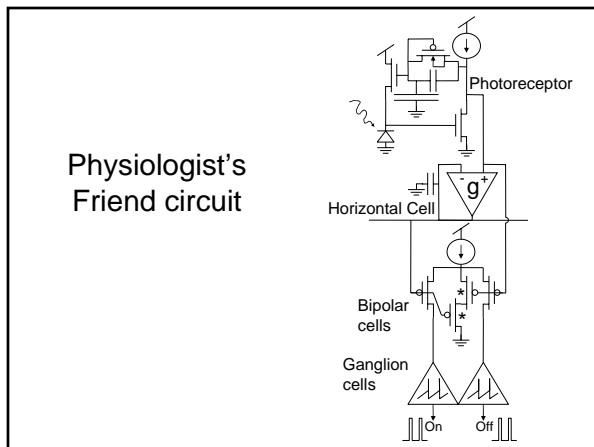
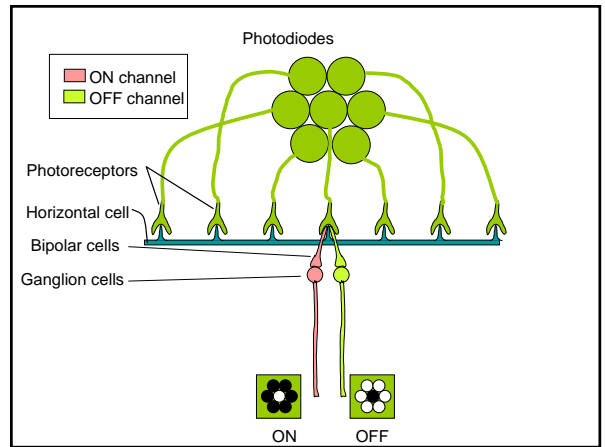
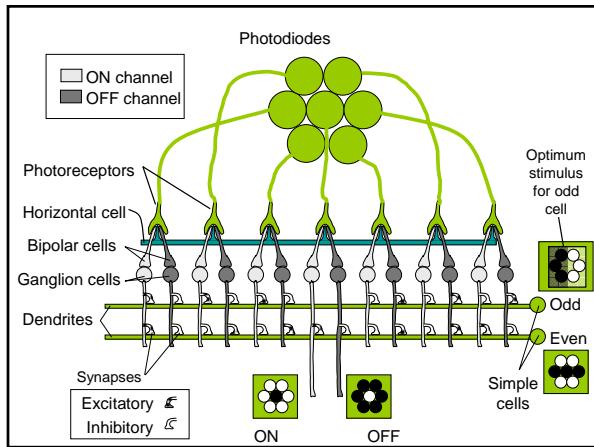
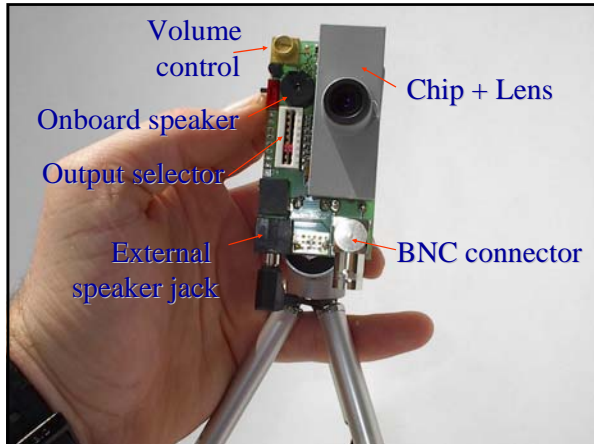
The “Physiologist’s Friend” chip

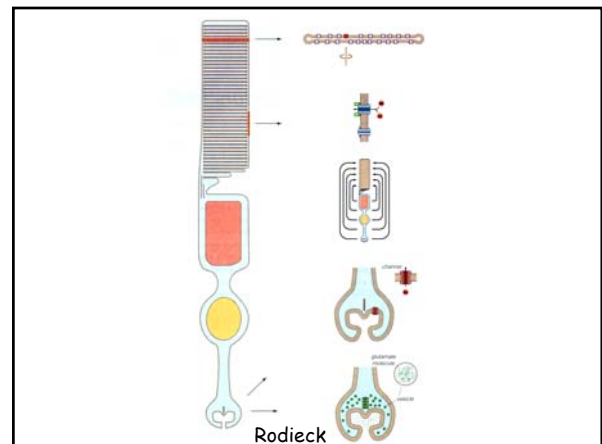
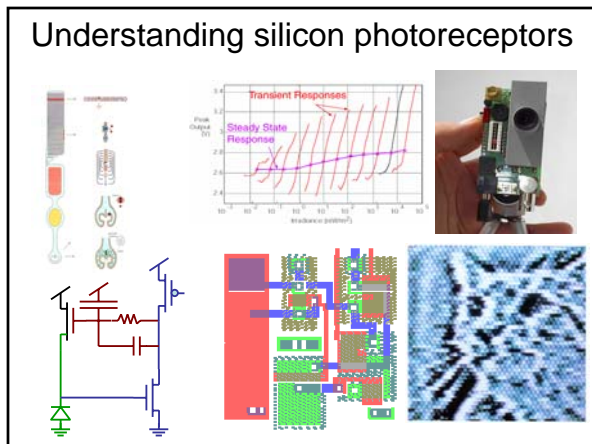
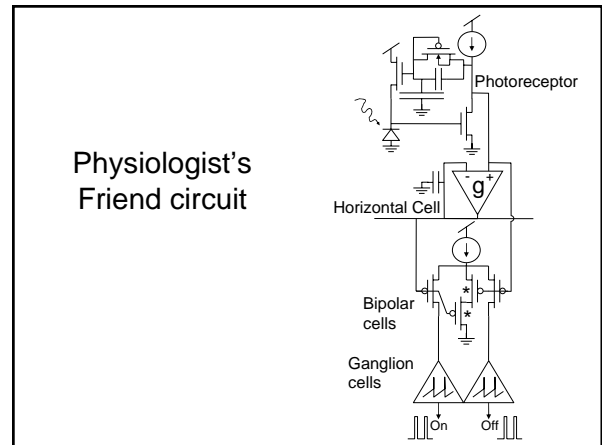
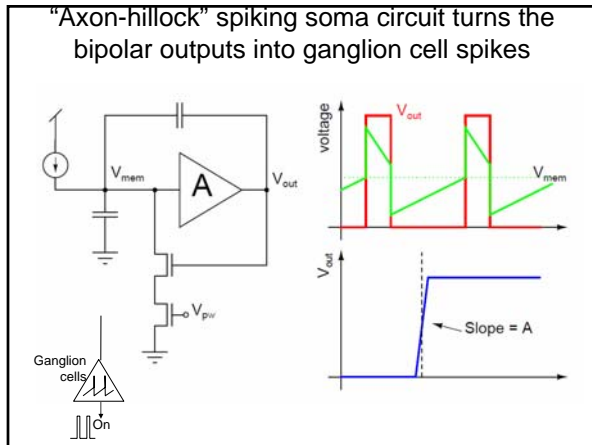
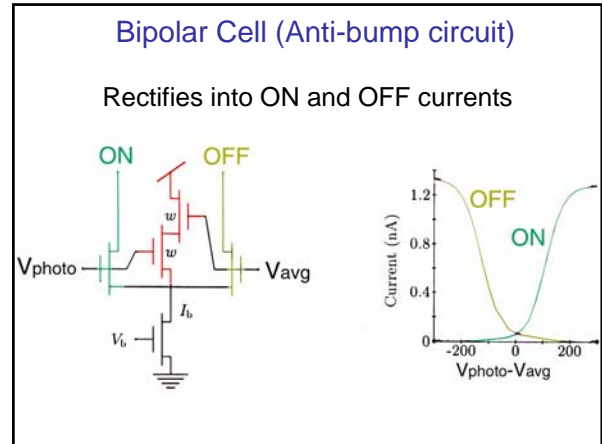
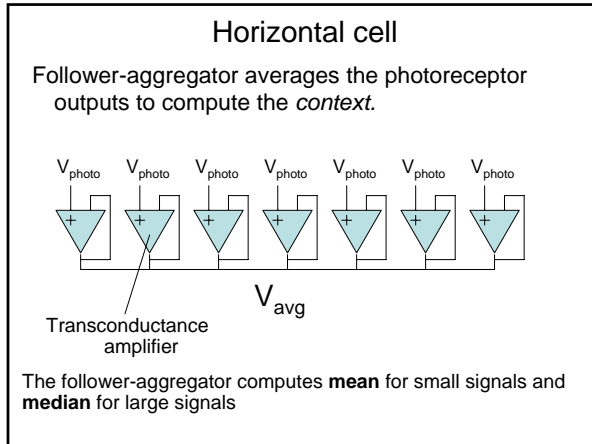
A Typical Visual Physiology Setup



Physio Friend Layout







Practical aspects of photodiode design

Drawing a photodiode

- You can use either *nwell* or *ndiff* as a photodiode in any CMOS process. It may be leaky and have low quantum efficiency but it will make photocurrent.
- Make sure you **block the salicide!**
- Parasitic photodiodes can kill you!** Any other junction will act as a photodiode unless you protect it from light and minority carriers.

Estimating photocurrent

- Good rule of thumb:
 1 lux = 10^4 photons/ $\mu\text{m}^2/\text{s}$ (Rose, 1973)
 - Moonlight 0.1 lux
 - Office light 500 lux
 - Sunlight 10^5 lux
- Average scene reflectance R is 18% (Kodak gray)
- Lux falling on chip is $1/8f^2$ imaged from white surface. f is aperture/focal-length
- Quantum efficiency is about 0.5

$$I_{\text{chip}} = \frac{I_{\text{scene}} R}{8f^2}$$

Dark current limits low-light performance

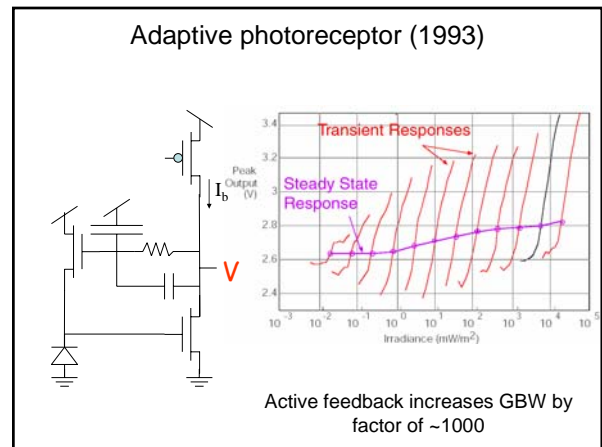
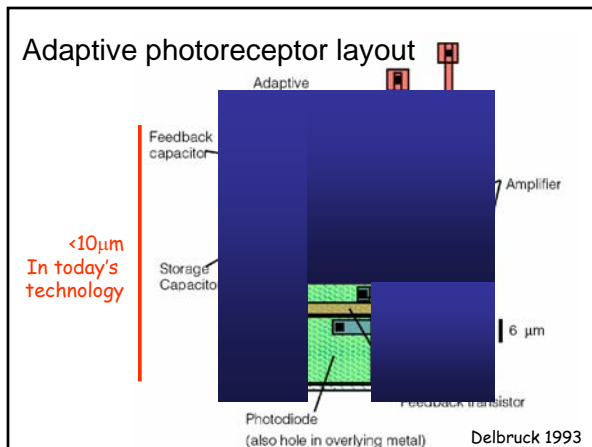
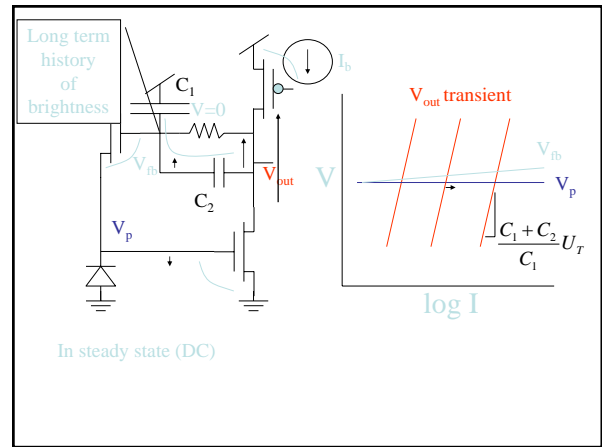
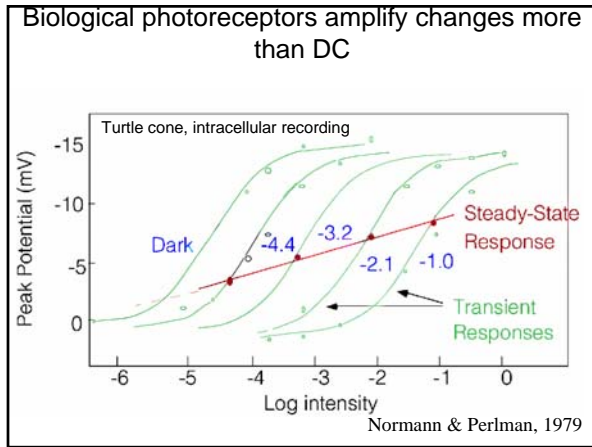
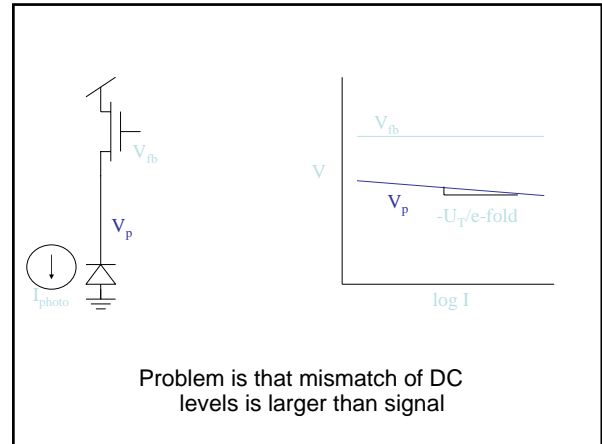
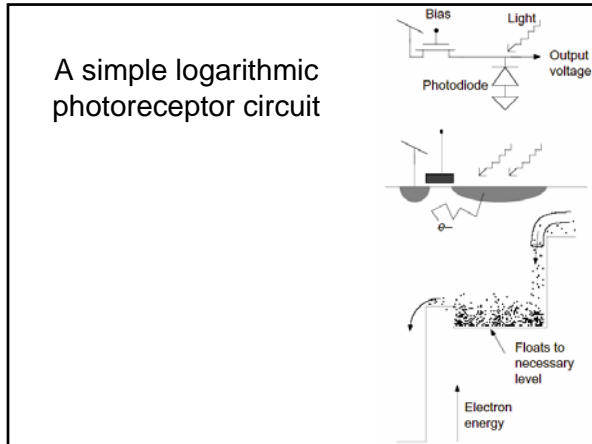
- Typical process leak $1\text{nA}/\text{cm}^2$ for large area junctions at 25°C
- Corresponds to about moonlight **scene** illumination
- Dominated by edges of junctions, where leakage is 10-100x higher: **red edge** leaks as much as **blue area**.
- Doubles every $\sim 6-8^\circ\text{C}$; from 25°C to 60°C increases 30X
- Is *expansive* nonlinear function of reverse bias (esp. for deep submicron processes)
- image sensor processes advertise 20-50x lower dark current, but these processes not available to usual multiproject services like MOSIS and Europractice
- Pinned photodiodes reduce even more, but have many restrictions, e.g. no nwell in pixel!

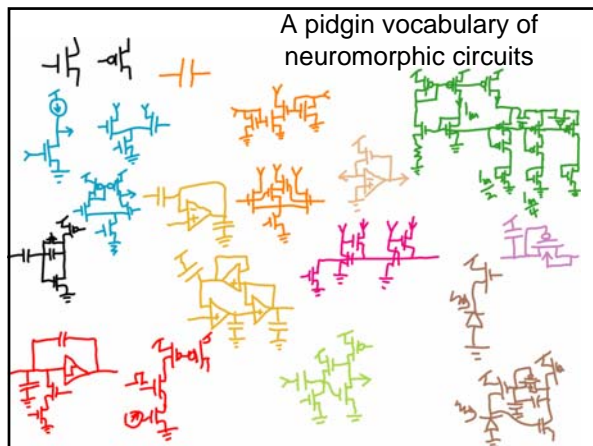
The *contrast* of reflective scenes is invariant to illumination

A logarithmic representation of luminance preserves reflectance

log is self-normalizing and automatically preserves reflectance differences

$$d(\log X) = dX/X$$





For more information, google "Tobi Delbruck" and look for wiki – follow links there



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Tobi Delbruck home page

My research at the [Institute for Neuroinformatics \(INI\)](#) in Zurich, Switzerland centers on y

I am an Oberassistent (Group leader) of the Neuromorphic Hardware group, along with [Shih-Chih Liu](#) and REEB, Secretary of IEEE CAS [Sensory Systems TC](#), coorganizer of [ISCAS 2006 Demo Session](#), [CAS](#)

Recent activity

- [Wiki: DLP lecture material](#)
- [Tobi Delbruck's website](#)

Apply to Telluride workshop!