Delbruck T, Berner R, Lichtsteiner P, Dualibe C: 32-bit Configurable bias current generator with sub-off-current capability. In ISCAS; Paris: 2010:(in press)

32-bit Configurable Bias Current Generator with Sub-Off-Current Capability

Tobi Delbruck[1], *Senior Member, IEEE,* Raphael Berner[1], *Student Member, IEEE*,
Patrick Lichtsteiner[1], *Member, IEEE,* Carlos Dualibe[2]
[1]*Inst. of Neuroinformatics, University of Zurich and ETH Zürich, Switzerland*, [2]*Freescale Semiconductor, Brazil*

ABSTRACT

A fully configurable bias current reference is described. The output of the current reference is a gate voltage which produces a desired current. For each daisy-chained bias, 32 bits of configuration are divided into 22 bits of bias current, 6 bits of active-mirror buffer current, and 4 bits of other configuration. Configuration of each bias allows specifying the type of transistor (nfet or pfet), whether the bias is enabled or weakly pulled to the rail, whether the bias is for a cascode, and whether the bias transistor uses a shifted source (SS) voltage for sub-off-current biasing. In addition, the current reference integrates a pair of voltage regulators that generate stable voltage sources near the rails, suitable for the SS current references. Measurements from fabricated current references built in 180 nm CMOS show that the reference achieves at least 110 dB (22-bit) dynamic range and reaches 160dB when power-rail gate biasing is included. Generated bias currents reach at least 30x smaller current than the transistor off-current. Each current reference occupies an area of 620x50 um^2. The design kit schematics and layout are open-sourced.

1. INTRODUCTION

Mixed signal chip designs sometimes require a wide range of internal currents for biasing. Sometimes during development these are controlled by gate voltages with the disadvantage of severe process and temperature sensitivity, and also supply voltage sensitivity if a stable reference is not used. Parts of the design may run at bandwidth or slew rates of 100MHz while others may run at 1Hz, requiring bias currents that span 8 decades. We previously reported bias current references for generating fixed bias currents [1] over this very wide range. Our experience showed that most chip designs could not be adequately simulated to allow for first-shot fixed biasing. We next developed a 24-bit digitally-programmable bias current generator [2] along with extensive PCB, firmware, and host software infrastructure [3]. Although successful on [4] and several other chips, we learned that these programmable biases placed strain on the designers by forcing them to correctly tie the proper nfet or pfet bias output to their circuit, and not allowing them to disable the on-chip biasing under software control, and not allowing control of the bias voltage buffer strength. Designers also often wished to tie biases to ground or Vdd explicitly. It proved necessary to still bring the bias voltages out to pads and provide external overriding capability at the board level. Also, given decreasing threshold voltage and consequent increase in transistor off current, we wanted to incorporate the notion of shifted-source (SS) biasing [5, 6] in a fully integrated form, to allow chips to utilize very small currents and long time constants without using off-chip voltage sources.

Here we extend this previous work to generalize the bias current reference to add full configuration capability. We also added the capability of generating sub-off-current values and the required voltage references and regulators to use these SS current sources.

In the rest of this paper we first review SS operation, and describe the new reference and regulator. We then describe the overall bias current architecture, and describe the new bias buffer circuit which supports full configurability. We conclude with characterization results and discussion.

2. SHIFTED SOURCE BIASING

In the following we use the term *off current* to mean the saturation current of a transistor with V_{gs}=V_{sb}=0, i.e. the pre-exponential I_0 in the saturated subthreshold transistor drain current: $I_{ds} = I_0 \exp(\kappa V_{gs} / U_T)$, where κ is the back-gate coefficient and U_T is the thermal voltage. I_0 is typically several orders of magnitude larger than the junction leakage substrate current. Normally a current mirror can only copy currents down to a few times I_0.

References [5, 6] presented the principle of SS biasing. The idea is to arrange to allow a current mirror to operate with its gate voltage below its common source voltage. A level-shifting source follower tied from the current mirror drain input to the common gate voltage V_g holds the drain-source voltage of the input transistor in saturation

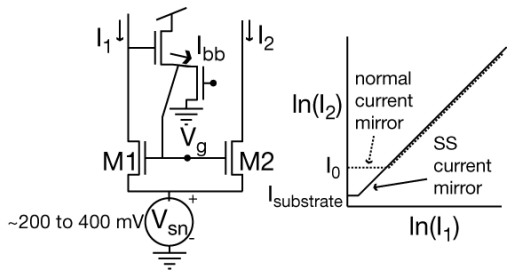

Fig. 1 Principle of shifted-source (SS) current mirror.

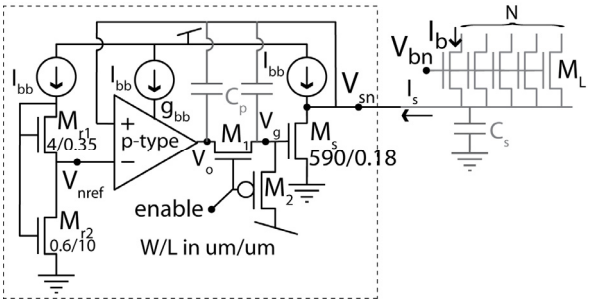

Fig. 2 Shifted-source reference and regulator circuit.

(Fig. 1) even for very small I_1. The common sources of both M1 and M2 are held at regulated voltage V_{sn} which is typically 200mV to 400 mV above ground. This SS allows V_g to drop below V_{sn} for very small (sub-off) input currents. The current mirror is then capable of copying currents several decades smaller than I_0. To build a complete system, complementary pairs of such mirrors are required with supplies V_{sn} and V_{sp}.

[5, 6] did not propose a means for generating or regulating V_{sn} and V_{sp}. The difficulty is that the required voltages are quite close to the power rails. We propose generating the V_{sn} regulated voltage with the low-dropout regulator circuit [7] in Fig. 2, with the complementary circuit for V_{sp}. The reference voltage V_{nref} is generated by the split-gate diode-connected pair M_{r1} and M_{r2}. M_{r1} is wide and short and M_{r2} is long and narrow. M_{r2} runs in triode mode, acting as a load resistance and thus allowing generation of a reference voltage of 200mV to 400mV. The programmable buffer bias current sources I_{bb} sets V_{nref} and biases the 5T p-type OTA error amplifier, which acts as an opamp. The wide pass transistor M_s sinks the current I_s supplied by the N external nmos sources M_L. The OTA drives V_g (when the regulator is enabled) in negative feedback to regulate V_{sn} to V_{nref}. If V_{sn} is too low then V_g is decreased, and vice versa. The I_{bb} current source onto V_{sn} holds V_{sn} up when I_s sourced externally becomes very small. It also sets the minimum transconductance of M_s. Switches M_1 and M_2 allow disabling the SS regulator and tying V_{sn} to ground by disconnecting the OTA and tying V_g to Vdd. Parasitic capacitances C_p (especially across the drain-gate capacitance of M_s) can lead to instability since they provide a positive feedback path from V_o to V_{sn}. A large C_s/C_p capacitive divider ratio reduces the feedback gain to stabilize the regulator.

3. BIAS GENERATOR ARCHITECTURE

We now describe the overall architecture of the bias generator. Fig. 3 is a block diagram showing the interface between an off-chip controller and a set of N independent bias currents, along with the architecture of a single bias. A master current I_m with PTAT characteristics which is generated by a single Widlar bootstrapped mirror [1] is shared over all N biases. This PTAT source has proved to be good for our applications, where we generally want constant-g_m performance from the subthreshold circuits. The 32-bit configuration word for a bias is shifted into shift register stages (SR) and then latched (L). It is partitioned into 22 bits for the bias current I_b, 6 bits for the bias buffer current I_{bb}, and 4 bits of other configuration. Biases are daisy-chained (15 in the case of the present implementation). Bits are loaded on the IN0 bit while clocking CLOCK; after all bits have been loaded, LATCH is toggled to activate new settings.

The configuration bits operate inside the bias buffer circuit BB (Fig. 4). This complicated circuit has many switches that enable various modes, but the principle of operation is simply based on a complementary pair of active SS mirrors as in Fig. 1. The flow of signal current is shown by the dashed arrows. The input to the buffer circuit is the programmed fraction I_b of I_m, and the output is a buffered bias voltage V_{bias}. Internal buffer currents are set by I_{bb}, which is derived from a 6-bit fraction of I_m. The configuration bits (DISABLE, CASC, SSEN, NBIAS and the global power-down bit PD) operate switches that switch in or out various parts of the circuit. For example,

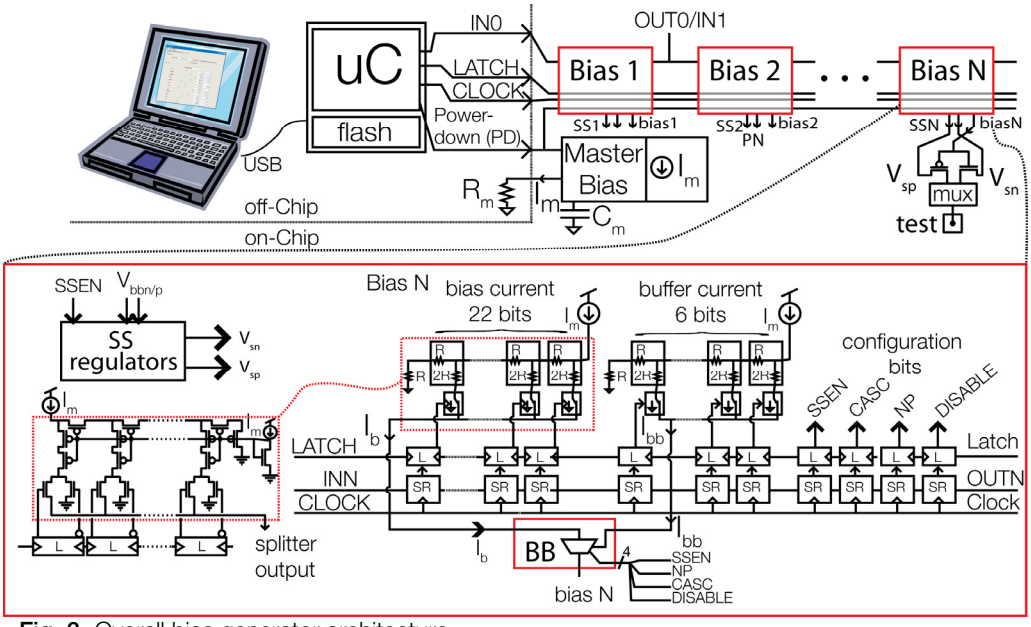

Fig. 3 Overall bias generator architecture.

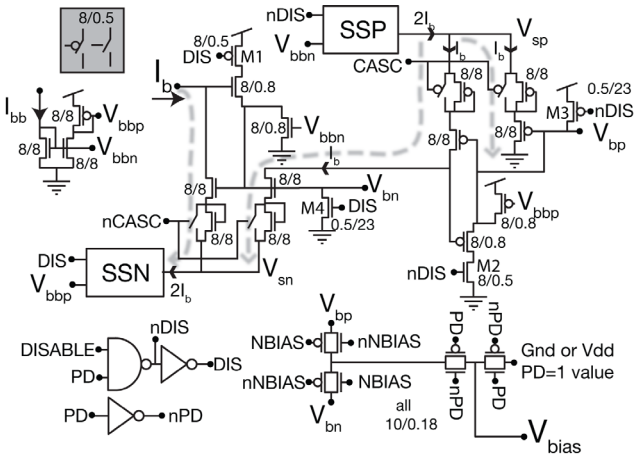

Fig. 4 Configurable bias buffer (BB) circuit.

if an n-type normal bias is desired with shifted-source voltage level, then DISABLE=0 enables the SS regulators, NBIAS=1 enables the n-type output, and CASC=0 shorts across the diode-connected loads in the active mirrors. M1 and M2 are added to prevent parasitic floating node states when the bias is disabled, where intermediate nodes can fight. M3 and M4 weakly clamp the bias voltage to the rail when DISABLE=1. The default state with PD=1 is set by tying V_{bias} to Gnd or Vdd in layout, which can be important for power-up state of the chip.

4. IMPLEMENTATION

This bias generator was implemented on a vision sensor in a 180nm 4M 2P MIM image sensor process (UMC CIS 180). Fig. 5 shows a partial micrograph of the chip with layout overlaid and a close up of the layout of the bias buffer/references/regulators layout. Each bias occupies an area of 620 um x 50 um=0.0033 mm^2, which is about 80% of a 200x200 um pad. To prevent parasitic photodiode action at low currents, the entire circuit is covered with image sensor black shield and low current parts of the circuit are covered with metal; pfets and nwell guard rings around nfets provide additional shielding.

5. CHARACTERIZATION

Bias currents were measured under GPIB computer control of a Keithley 6430 source-measure unit. An on-chip nfet and pfet were included with common gate tied to one of the generated biases and drains brought to pads (Fig. 3). The sources are tied to the on-chip V_{sp} and V_{sn}. One V_{sp} was also brought out. These test transistors were sized with relative strength of 500 and 625 for n and p type transistors, respectively. These large W/L's allows indirect measurement of very small on-chip bias currents. Current measurements have been corrected by the estimated multiplier ratio.

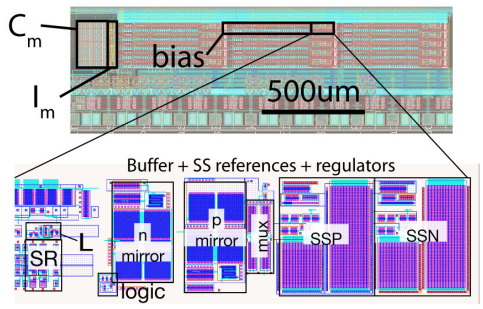

Fig. 5 15-bias micrograph from corner of die overlaid with layout and with close up of BB and SS layout.

The master current I_m was set to 1.3uA by external resistor R_x=100kΩ. I_m was directly measured through R_x. The largest generated current is predicted to be $I_m/2$ and the smallest generated current is predicted to be a factor of 2^{22}=4M times smaller than I_m, or about 310fA. The measured currents are approximately linear with bias code value (Fig. 6a) except for large values of current where they increase more slowly than predicted. This is expected from the differing super-threshold behavior of the wide/short test FETs and the 8um/8um BB FETs and the intervening current multiplexor. The measured off currents I_{0n} and I_{0p}, corrected by the same scale factors as the measured currents, are about 3pA. Using SS biasing, the smallest measurable generated currents go down to about 300fA, a factor of 10 smaller, and consistent with the 22-bit resolution of the splitter. Additional testing using a larger R_x=390kΩ (resulting in a smaller I_m=0.22uA) shows a minimum measurable current using SS biasing of about 100fA. By setting an opposite-type bias (e.g. enabling p-type bias for an nfet) or by tying the bias to a rail, higher currents can be obtained; the maximum possible current at Vdd=1.8V is about 15uA from a square nFET in this process, giving a total dynamic range of roughly 160dB. Fig. 6b shows matching across 7 chips, reflecting inter-die threshold voltage mismatch. This constant relative variability (in the lower current

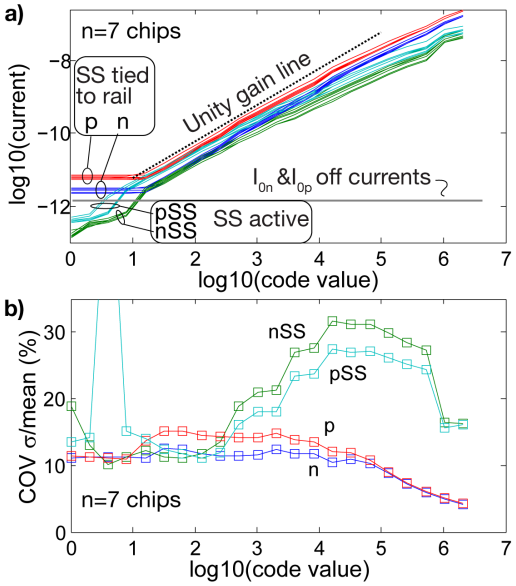

Fig. 6 a) Measured bias currents vs. bias code value. b) Measured coefficient of variation (σ(I)/I) across 7 chips.

region) at any node of the current splitter is a consequence of the fact that series and parallel resistors combine to have the same total variability as any single element [8]. The lowest variability is obtained from an n-type non-SS bias at low current. The higher variability at higher currents, using p-type, or using the shifted sources, probably arises partly from the BB circuits and the readout pathway.

Results from the SS V_{sp} regulator are in Fig. 7 and Fig. 8. The effective DC resistance of the regulator is about 100Ω, which is sufficiently small since typically the M_L currents that supply I_s (Fig. 2) are constant and only a stable V_{sn} and/or V_{sp} are required. The time constant of recovery of V_{sn} and V_{sp} from a perturbation depends on the load capacitance; with a 10uF bypass capacitance nominal on-chip bias current values of 1nA, the small-signal recovery time constant is on the order of 2ms. The large-signal perturbation in Fig. 8 exposes the rapid recovery from negative perturbations and the slewing recovery from positive perturbations.

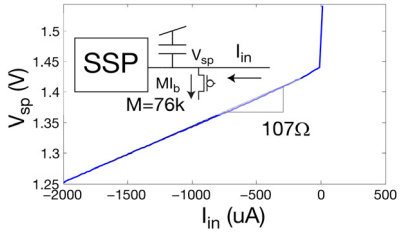

Fig. 7 Measured SS regulator DC regulation. V_{sp} vs. I_s is shown relative to Vdd, for midrange setting of I_{bb}.

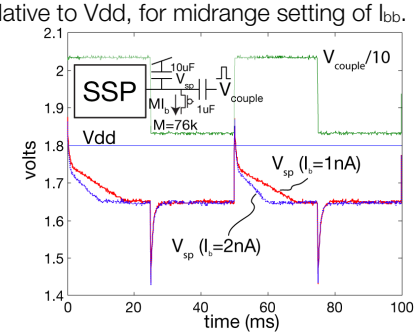

Fig. 8 Measured SS regulator AC regulation. V_{sp} is shown when a square wave V_{couple} is capacitively coupled into it.

6. DISCUSSION

Fig. 9 summarizes specifications. The tested implementation is fully functional. The next generation will enhance on it as follows: To speed up bias modification over the external serial link from the ~150us of the current version, the biases will be individually addressable. Instead of generating a pair of SS voltages for each bias, a single programmable pair will be shared over all biases. We may use a coarse-fine strategy or compound mirrors to increase the dynamic range still further.

To promote the use of on-chip biasing and speed up fully-integrated chip development, a design kit for this bias generator including schematics and layout has been open-sourced in the jAER project [3] which also includes PCB layout, firmware and host software. The design kit is free and has relaxed (LGPL-like) licensing terms. We hope these efforts will help bring silicon to more convincing realization.

Technology	180nm 4M 2P CIS
Supply voltage	1.8V
Master current area incl. C_m	220um x 260um
Per bias area	620um x 50um=0.0033 mm^2
Bias dynamic range, not incl. power rail saturation	22 bit fraction of I_m=110dB
Bias buffer range	6 bit fraction of I_m
Configuration bits	4 per bias
Weak disable Idsat	p-type: 2uA; n-type: 12uA
Current consumption per bias	~4I_m
SS regulator resistance	110 ohms
Total range incl. Vdd or Gnd bias	160dB
Min current with I_m=1.3uA	360fA
1-σ p-type low-current-mode variation of measured bias currents	12%, n=7 dies.

Fig. 9 Specifications

7. ACKNOWLEDGEMENTS

Supported by ETH internal funding TH-18 07-1, Swiss National Science Foundation grant 200021-112354/1, the Univ of Zürich, and ETH Zürich.

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