# Pulsed bipolar CMOS imager

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## Abstract

This paper will describe an active pixel CMOS-compatible imager aimed at high resolution still cameras.

We will discuss pixel operation, column sense circuits, serial output, and show results from existing imagers. In this abstract, we show results from a prototype 640x480 imager with 5.9x5.9 $\mu m^2$ pixels built in 0.8 µm double-poly CMOS with one additional base implant.

## Active Capacitor-coupled Bipolar Pixel

The pixel (Fig. 1) is a vertical NPN bipolar transistor with floating base capacitively coupled to common row lines, common collector, and emitter tied to common column lines. The base is reverse-biased to collector and emitter during integration. For readout, a strobe pulse is capacitively coupled to the base, forward-biasing the base-emitter junction, and dumping the bipolar-amplified base charge onto the emitter. Readout happens row by row; while each row is strobed and its pixel's charge output is sensed by column charge-sense circuits, the previous row's output is serially scanned out.

Fabrication of the bipolar active pixel is CMOS compatible with one additional mask for p-base implant (inside n-well). The dielectric of poly to base capacitor is formed by the gate oxidation. The base capacitor is not sensitive to misalignment between poly and diffusion masks. The emitter n+ implant is self-aligned by the LDD structure and n+ S/D implant. The NLDD implant reduces leakage current at the emitter-base junction and reduces bipolar action along the emitter edge. The entire pixel array shares a common n-well collector tied to Vdd.

The pixel charges in a row are dumped onto the column lines by strobing the row line momentarily high (Fig. 2). The strobe signal is generated off-chip during the sense phase of the column charge sense amplifier. This strobe signal is routed to a particular row by vertical scan circuits.

The periodic pixel strobing pushes the instantaneous base current up to a level where β does not suffer low-current degradation. The peak pixel current is hundreds of times higher than it would be if the transistor were operating continuously in a forward-biased state.

The strobe line capacitive coupling to the base, $C_{sb}$, determines the saturation charge $Q_b$ that can be dumped from the base

$$Q_b=\Delta V_{strobe}C_{sb} \quad (2)$$

Fig. 1. Schematic, layout, and cross-section view (vertically not to scale) of the new bipolar active pixel with capacitor coupled base. The fabrication process is CMOS compatible with one masking step for p-base implant (inside n-well).

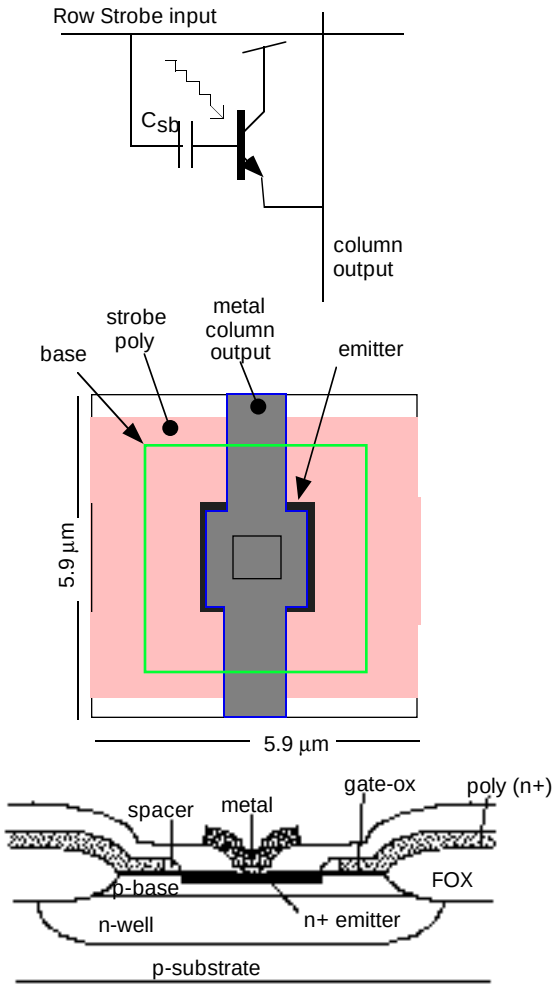
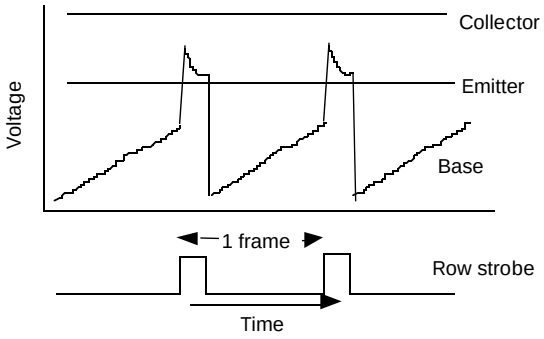


Fig. 2. Pixel dynamics




Dark current in the reverse-biased pixel junctions, especially nonuniform dark current (hot spots) limit the lower end of operation. Dark current is caused by thermal photons. Defects that result in mid-band states greatly increase dark current, resulting in hot spots.

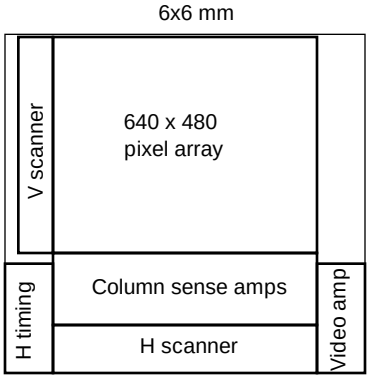
## Imager architecture

The imager floorplan in Fig. 3 shows the arrangement of pixel array, column amplifiers, and miscellaneous circuits. This architecture is familiar from other CMOS imagers.

## Column Circuits

At the bottom of each column is a charge sense amplifier. The pixel outputs from a row are sensed in parallel by the amplifiers at the bottom of each column. After sensing, the results for each column are sampled and held during the horizontal blank period. While the next row of pixels is being sensed, the last column's data is scanned out serially. A simplified schematic of the column charge sense amplifier is shown in Fig. 4.

Fig. 3. Imager floorplan

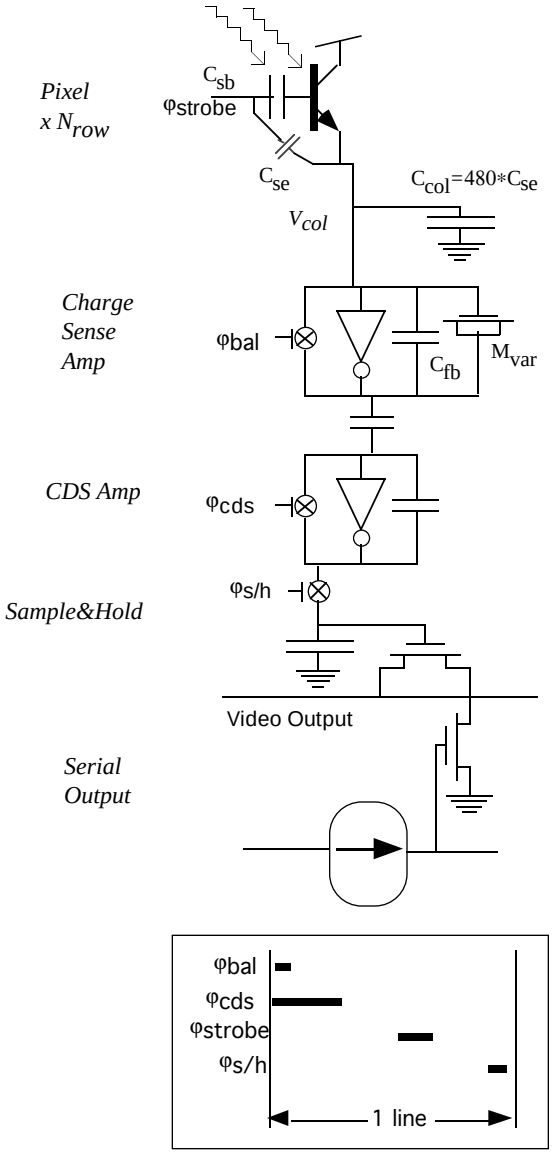



The first amplifier senses the charge. The second amplifier has unity gain and is used for correlated double sampling. The sense amplifier feeds into the correlated double sampling amplifier, which feeds into the sample and hold, which controls the video output transistor.

Column circuit design is constrained to be simple by the narrow column pitch. Fig. 4 may be realized in the space for 1 metal wire to pass by 1 contact in each column.

A fixed small capacitor $C_{fb}$ and a varactor $M_{var}$ are connected between the input and output of the amplifier. These capacitors set the sensitivity of the amplifier to charge dumped onto the column line from the pixel.

Fig. 4. Column charge sense circuits



The open-loop gain of the amplifier is 5–10 times larger than the ratio of the column capacitance to the feedback capacitance, to make the charge dumped onto the column appear across the column capacitance and not across the feedback capacitance. A large open-loop gain keeps the input to the charge sense amplifier clamped, so the column charge must appear across the sense capacitor.

In addition to the fixed feedback capacitance $C_{fb}$ in the charge sense amplifier, there is a varactor $M_{var}$. The varactor is an nMOS capacitor with channel tied to amplifier output and gate tied to column. As more charge is dumped onto the column, the charge sense amplifier output drops. Eventually the nMOS channel turns on, greatly increasing the feedback capacitance and hence reducing the gain. Using the varactor increases dynamic range by at least a decade. Perhaps more important, it provides a graceful highlight saturation behavior.

The second amplifier in the column amplifier does correlated-double-sampling, by computing the difference in the sense amplfier output before and after strobing charge out of the pixel. This correlated double sampling is necessitated by thermal *kTC* charge fluctuation on the column line during sense amplifier reset. The RMS fluctuation is about 800 e- for a 4pF column.

The only circuit elements that contribute DC voltage offsets to the column outputs are in the CDS amplifier and the video output transistor. All previous circuit elements contribute no DC offset because they are capacitively coupled to the CDS amplifier. We sized the critical transistors as large as practical to minimize these offsets.

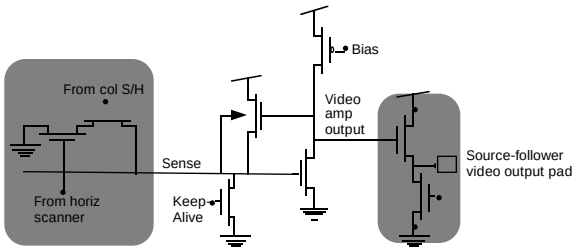
## Serial Video Output

While the next row of pixels is being sensed, the previous row's sampled column amplifier outputs are scanned out serially by sequentially sensing the currents produced by the video output transistors (Fig. 5). These transistors are turned on sequentially by a horizontal shift register circuit that shifts a single bit along the bottom of the array. The current from one column is sunk from global video output line, and is sensed by the fast transimpedance amplifier. A source-follower buffers this signal offchip, where additional video conditioning is performed by commodity video amplifiers. This video output chain is nearly unity-gain.

The feedback in the video amplifier clamps the voltage of the video output line, effectively speeding the response. Simulations show that the video amplifier has a gain-bandwidth product exceeding 200MHz. The rise-time is less than 10ns.

A keepalive transistor sinks a constant current from the video sense line to keep the video amplifier feedback biased during horizontal blank. This keepalive current reduces the transient at the start of each line.

Fig. 5. Onchip video amplfier.




A new bit is loaded into the horizontal shift register automatically when the old one has been shifted out of the end. A wired-OR holds the summing node low whenever a bit is in the register. When the bit falls out, a new bit is generated. To allow offchip synchronization between multiple imagers, an additional NAND at the input to the register serves to hold off any bits from being loaded. Additional wired-OR circuits generate the video blank and sync signals used to drive an analog monitor display.[5]

Vertical timing and column amplifier clocking is generated by an offchip microcontroller.

## RGB color camera

We jury-rigged an RGB camera (Fig. 6) with 3 imager chips and dichroic color separation optics from an obsolete broadcast-quality Saticon tube television camera. We mounted the chips in place of the tubes and clocked them in parallel using a single microcontroller. We didn't use any color correction filters over the imagers.

Using separate imagers for RGB is optimal because it completely eliminates color aliasing introduced whenever a filter matrix is used with one chip. It also has the virtue of avoiding fabrication of the filter mosaic. Each imager can be indepen-

Fig. 6. RGB camera

dently focused, so chromatic aberrations are minimized. Alignment proved difficult, so we optimized rotational alignment and post-processed the images to shift the color channels into alignment.

## Performance

Resolution was nearly determined by the number of pixels, despite pixel size 5.9µm and marginal optics. Fig. 7 shows an RGB image of a resolution chart along with a blowup.

Fig. 8 shows saturation characteristic due to varactor feedback in the sense amplifier.

Measurements indicate dark currents around 5 nA/cm$^2$, equivalent to an exposure of about 100 e- in 1/60 second. This value is larger than acceptable by a factor of at least 10, more like 100. Improved process technology, modification of base-emitter doping profiles, etc., should reduce this value significantly.

The entire test board runs on about 95mA with a 5V supply. The board itself (pots, LED) takes 40mA, the PIC microcontroller takes about 15mA, video output (75 ohm driver) takes 5mA, and the imager takes 35mA.

## Discussion

The full paper will present extended characterization from imagers presently in fabrication that are based on the prototype shown here.

## References


(1) Carver Mead, "Integrating photosensor and imaging system having wide dynamic range with varactors", US patent 5,260,592, Nov. 1993.
(2) A. Bergemont, M. Chi, H. Haggag, and C. Mead, Patents pending, 1996.
(3) C. Mead, "Sense amplifier", US patent 5,276,407, 1994.
(4) C. Mead and F. Faggin, "Integrating imaging system having wide dynamic range with sample-and-hold circuits", US patent 5,324,958 1994.
(5) C. Mead, T. Delbruck, "Scanners for visualizing analog VLSI circuits", Caltech memo. *http://www.pcmp.caltech.edu/anaprose/tobi/scanners/*, 1991.


Fig. 7. Resolution chart, with close-up

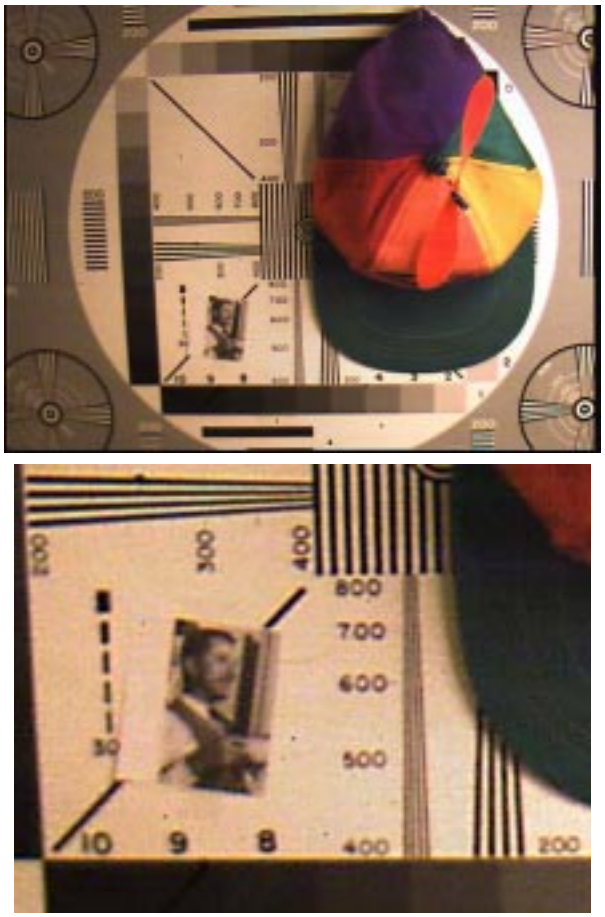


Fig. 8. Varactor effects. (Top) Log test chart under bright illumination, lens set at f/1.4, shutter speed 1/50s. Peak illumination is about 10EV@ASA100. Minimum luminance about EV5.5. Plot shows profile along bottom steps. Varactor compresses top end. (Bottom) Same except aperture decreased about 3 stops (factor of 8). Upper end of response no longer compressed by varactor.