A note on Tspice simulation of the MOS-bipolar adaptive element (tobi element).

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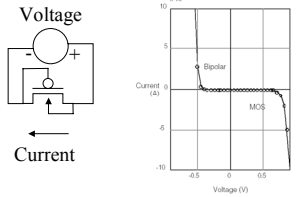
If you want to use Tanner T-Spice to simulate the adaptive element (shown to right) as used in the adaptive photoreceptor, consisting of a single PFET wired up to be a MOS in one direction and a diode/bipolar in the other direction, then you need to set appropriate values for the parasitic junction diodes in the PFET MOS transistor. If you don't, you will get a very misleading behavior that will result in non-physical circuit behavior. What I have seen is that the photoreceptor will simply not adapt, even though there is more than a volt across the adaptive element. The default in the Level 49 (BSIM 3v3.1) model is to turn off these parasitic diodes by setting the parameter **js** to 0. This parameter specifies the source/drain junction reverse saturation current density.



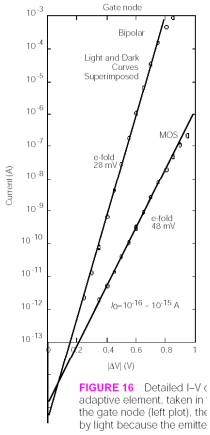
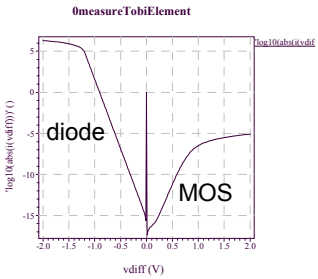


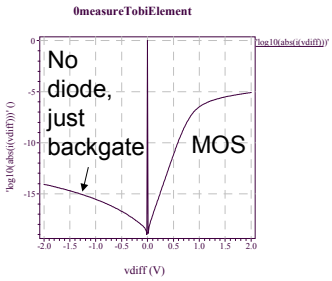
FIGURE 16 Detailed I–V c adaptive element, taken in the gate node (left plot), the by light because the emitte

js is the reverse saturation current in A/m^2. The junction dark current is about 1nA/cm^2 across most processes. **To make a reasonable model of this device, add the parameter js=1e-5 to the parameters of the PFET model.** (1nA/cm^2*10^{4}cm^2/m^2=1e-5A/m^2). (I have not bothered to set the sidewall leakage or the reverse leakage current terms, because I just want the correct qualitative behavior.)

At the right I compare the T-Spice DC transfer V-I curves without and with the **js** parameter. The x-axis is the differential voltage; the y-axis is $\log_{10}$(abs(I)). Note the sign of the differential voltage is flipped compared with the first figure; the MOS direction is on the right in the traces below. The log slope should be higher for the diode/bipolar action; this direction should e-fold approximately every 25mV, while the e-fold for the diode-connected MOS action should be about 40mV. When you don't have junction diode turned on, all you get in the diode/bipolar direction is the back-gate action of the MOS surface channel.



With junction diode



Without junction diode

Turning on the junction diode makes the asymmetry of the responses qualitatively correct. A measurement using the cursor shows that the slope of the MOS direction is too low, however; it should be about 100mV/decade, corresponding to a transistor back-gate coefficient κ of about 0.7, but it is modeled as a slope of about 72mV/decade, corresponding to an unrealistically high κ of about 0.9, which is absurd for a PFET operating at 0 bulk-source voltage.

The same simulated data for the tobi element is compared to the right. You can see that the MOS behavior is pretty non-physical. Well, that's SPICE…