Photo-ASICs: Integrated circuits for optical measurements using industrial CMOS technology

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Abstract

Cost-effective single-chip smart photosensors (photo-ASICs) have a wide range of applications in optical metrology systems. They may be realized through the integration of light-sensitive structures together with analog and digital electronic circuitry using a standard silicon process. Different optical sensing devices to be used as elements of such photo-ASICs were fabricated in an industrial CMOS process. Their electrical and optical performance proved to be surprisingly good.

1. Introduction

It is a well-known fact and sometimes a nuisance that semiconductor electronic circuits are photosensitive. This effect can be exploited by integrating light detectors with analog and digital circuitry on a single chip to realize smart optical sensing ICs, adapted to desired measurement purposes, which we call "photo-ASICs". In order to keep costs low and make use of analog and digital cell libraries, an industrial silicon process is preferable for photo-ASIC fabrication. While vertical junction diodes are the most obvious detectors [1] to integrate, the present work also explores other kinds of photosensitive structures suitable for practical optical measurement applications.

Today's dominant fabrication process for high-performance, cost-effective VLSI circuits is CMOS technology. For this reason we investigate the suitability of an industrial 3-μm CMOS process, namely SACMOS 3 made available by FASELEC Corporation, Zürich, for photo-ASICs. This is a single-metal, single-poly process with self-aligned contacts, which is illustrated by the inverter cross-section shown in Fig. 1(a). Various types of vertical photodiodes, a lateral photodiode, a PSD (position-sensitive device), linear surface-channel and buried-channel CCDs (charge-coupled devices) and a BBD (bucket-brigade device) have been designed, fabricated in MPWSs (multi-project wafer services) at low cost, and characterized electrically and optically.

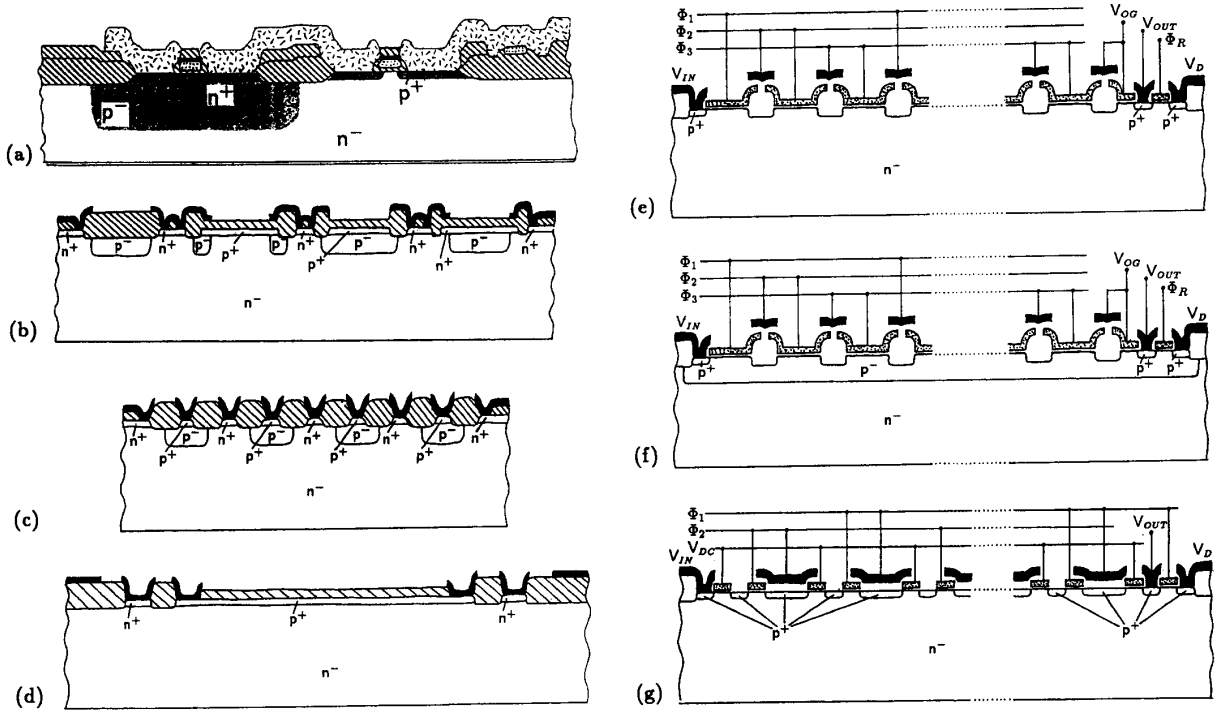

Fig. 1. Cross-sections of integrated devices in a CMOS process. (a) Inverter, (b) Vertical photodiodes, (c) Lateral photodiode, (d) Position-sensitive device (PSD), (e) Surface-channel CCD, (f) Buried-channel CCD, (g) Bucket-brigade device (BBD).

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2. Photodiodes

Four different vertical photodiodes have been fabricated with an area of 0.1 mm × 0.1 mm each, as shown in Fig. 1(b). They all exhibited external quantum efficiencies between 50% and 80% in the visible and near infrared. Their sensitivity spectra show some oscillation structure due to optical interference effects at the passivation interfaces, as can be seen in Fig. 2 for the p^- n^- diode. Surface leakage currents were found in the $n^+p^-n^-$ structure reducing the open loop voltages at all light levels and the short circuit currents for strong illumination. This was successfully avoided in the p^+n^- diode through the use of a p^- guard ring. Dark currents in the range of 1 pA were measured at room temperature. Rise-times of around 150 ns make these devices suitable for optical measurements at frequencies of several MHz. The lateral photodiode (Fig. 1(c)), in which the width of the space-charge region can be adjusted electrically, exhibits the expected change of effective photosensitive area; however this effect is restricted to about 5% without additional masking or post-treatment of the chip.

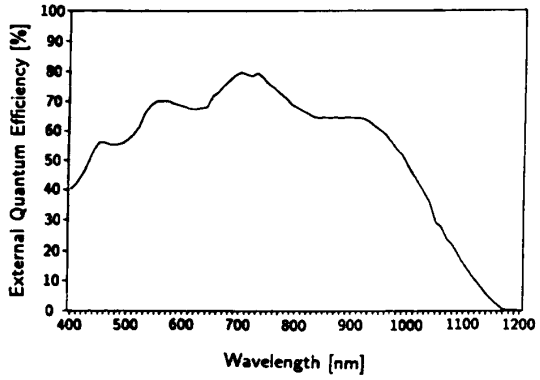

Fig. 2. Spectral dependence of the external (total) quantum efficiency of typical CMOS p-n-photodiodes. Note the spectral oscillations due to optical interference effects at the passivation interfaces; these can be reduced by applying an anti-reflection coating.

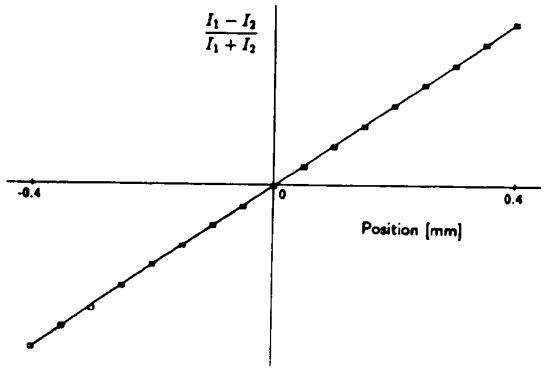

Fig. 3. Linearity of the PSD's position response. This graph of the PSD's electrical response vs. the true, mechanically measured position of a small light spot shows a standard deviation from perfect linearity of better than 0.5% in the central part (0.8 mm out of 0.9 mm) of the device.

3. Position-sensitive device

The lateral-effect photodiode shown in Fig. 1(d) is formed by a low-resistivity p^+ layer contacted at opposite edges and the n^- substrate. The device is 0.9 mm long (from electrode to electrode) and 0.1 mm wide. Because of the omission of a p^- guard ring the open loop voltages were much lower than for the vertical p^+n^- diode described above. The performance as a one-dimensional PSD proved to be very good: The position signal, i.e. the ratio of the difference and the sum of the output currents at the electrodes, generated by a small light spot scanned across the device showed a standard deviation from linearity of better than 0.5% (Fig. 3) in the central 0.8 mm of the device, approaching that of commercial PSDs.

4. Charge-coupled devices and bucket-brigade device

The CMOS process employed is not optimized for the fabrication of CCDs and BBDs, since only one polysilicon layer is available, the silicon-oxide interfaces may not be perfect, and the substrate is n-type. Nevertheless different linear charge transfer structures have been designed and characterized.

A surface-channel CCD consisting of 15 polysilicon electrodes (36 μm × 36 μm area each) with two-level three-phase clock is depicted in Fig. 1(e). Charge transfer was observed in this device, the clocks operating at 6.6 kHz between -22 V and -37 V with respect to the substrate. However, the charge transfer efficiency (CTE), i.e. the ratio of the charge transferred from one electrode to the next to the charge originally present in the packet, was strongly dependent on the signal level, with typical values between 95% and 98%. When carriers were only generated in a single potential well, either through a pulse at the input diode or through illumination of the corresponding electrode with a modulated LED, the amount of charge detected in the subsequent potential wells did not depend on the size of the original charge packet, as long as it was large enough to deliver this charge. This suggests the presence of a certain number of surface states, which trap carriers and re-emit them partly into the subsequent charge packets. This problem was solved by applying the "fat zero" technique, which means the introduction of a fixed bias charge into each packet in order to keep the surface states permanently occupied and thus to avoid the trapping of signal charge. With a constant bias of -0.75 V at the input diode and clock levels of -11 V and -26 V the CTE increased to 99.8%.

Operation of the buried-channel CCD shown in Fig. 1(f) has not been successful yet. This is probably due to the relatively high doping concentration of the p-well requiring a very strong reverse bias for full depletion. Another problem might be the presence of local potential minima beneath the inter-electrode gaps leading to incomplete charge transfer [2].

The BBD represented in Fig. 1(g) features 16 metal electrodes (32 μm × 36 μm area each) and polysilicon gates with a two-level two-phase clock and d.c. biased polysilicon gates separating neighboring electrodes [3]. The measured CTE was slightly over 96% with the clocks run between -11.5 V and 3.5 V at 6.6 kHz and the d.c. biased gates held at -6.5 V.

5. Applications

The possibility of realizing photodiodes with arbitrary shapes offers interesting opportunities in optical measurements. All linear transforms

$$L_f = \int_a^b I(x)\, f(x)\, dx \qquad (1)$$

of a a one-dimensional intensity distribution $I(x)$ with an arbitrary real weighting function $f(x)$ can be "calculated" optically at very high speed with two diodes: The first diode has a width $f^+(x)$, with

$$f^+(x) = \begin{cases} f(x) & \text{if } f(x) > 0 \\ 0 & \text{else} \end{cases}$$

thus representing the positive part of the weighting function. The second diode has a width $f^-(x)$, with

$$f^-(x) = \begin{cases} -f(x) & \text{if } f(x) < 0 \\ 0 & \text{else} \end{cases}$$

representing the negative part of the function. Subtraction of the two output signals then yields the linear transform as

$$L_f = \int_a^b I(x)\, f^+(x)\, dx - \int_a^b I(x)\, f^-(x)\, dx \qquad (2)$$

A simple example of this general technique is a 3-D sensor based on a triangulation principle called light-sectioning, where the three-dimensional shape of an object surface is measured from profile lines appearing at the intersection of the surface with a sheet of light. The evaluation of these lines requires their segmentation and the detection of the lateral optical centroid of each segment. This may be accomplished either by a linear array of PSDs [4] or by a linear array of wedge-shaped photodiodes [5,6], where $f(x) = a \cdot x$, as illustrated in Fig. 4. Arrays of photodiodes with non-standard shapes can also be used to detect certain symmetries in light distributions and for focus sensors [7].

CCDs and BBDs have a variety of applications in the signal processing domain, employing only small numbers of stages, where the demands on the CTE are consequently not as high as for imaging devices. These include delay lines, various types of time-domain filters, correlators, etc. [8].

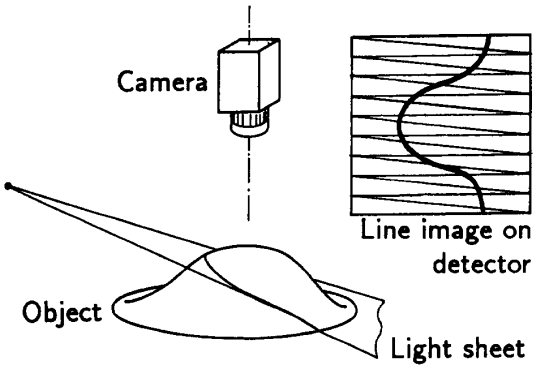

Fig. 4. 3-D sensor consisting of a linear array of wedge-shaped photodiodes for the fast optical determination of the local lateral centroids of a light profile.

6. Discussion

Most of the considered devices perform well enough to be employed as photo-ASIC components. Notable are especially the high quantum efficiencies of the photodiodes (which might be enhanced through the use of AR coatings), the good linearity of the PSD and the CTE of the surface-channel CCD, which meets the requirements of many signal processing applications. This shows that even an inexpensive MPWS with a CMOS process offers a variety of opportunities for the fabrication of photo-ASICs. This is useful for the production of low-cost devices in small quantities. A second polysilicon layer, however, may be essential for the operation of buried-channel CCDs.

In addition, hybrids of silicon and compound semiconductors (used for tuned light-sources) may soon make feasible complete optical measurement systems in single IC packages.

7. Acknowledgements

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8. References

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